Doc. Version	0.1
Total Pages	30
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Product Specification
3.6″ COLOR TFT-LCD MODULE

MODEL NAME: A036QN02 V0

<◆>Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	22/Jul/2005		First draft.
0.1	08/Sep/2005	3 6-7 9-13 15-16 17 18 20 21	A036QN02 V0 only support CCIR-656, and serial 8bit. RGB Modify I/O descrption Modify register default value Correct application circuit Delete Note 2 of 3.5.1 Correct 3.5.1.3 (a) figure, and delete (b). Add item “Vsync to 1st active line” of 3.5.2.1 Add “3-wire serial communication AC timing” figure

Contents

General Description

A036QN02 V0 is a amorphous transmissive type TFT (Thin Film Transistor) LCD (Liquid crystal Display). This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), and backlight unit.

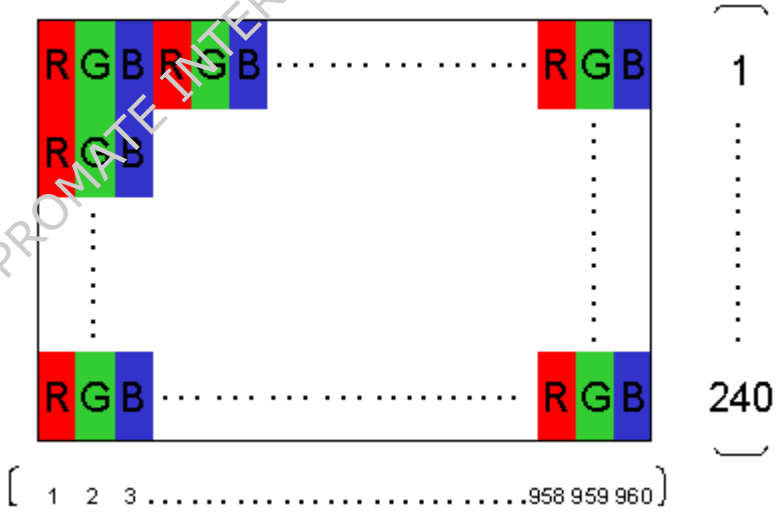
Features

- 3.6-inch display size
- QVGA resolution and stripe dot arrangement
- Premium SIA (**S**mart **I**ntegration **A**dvance). Support below functions
  - Video brightness adjustable
  - Video contrast adjustable
  - Backlight current adjustable
  - Gamma adjustable
  - Hue adjustable
- Built in timing controller and two DC-DC controller
- Single 3.3V power supply
- Standby mode supported
- VCOM amplitude selected
- 3-wire register setting
- Low power consumption
- Various interface support:
  - CCIR-656;
  - Serial 8-bit RGB
- NTSC and PAL standard supported
- 2-in-1 FPC
- Wide viewing angle
- Slim 3.22mm thickness design
- Green design

1. General Information

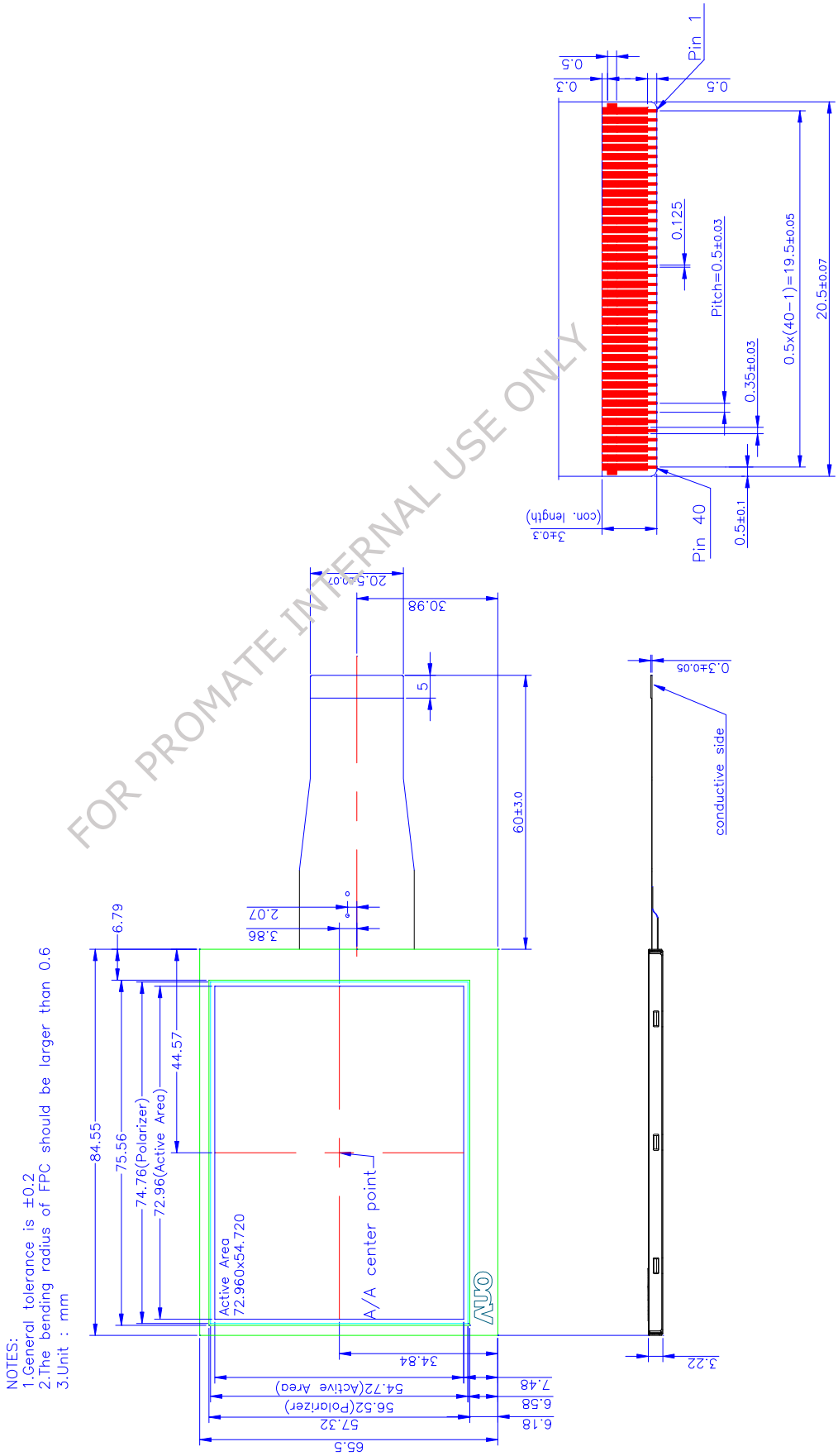
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	960(H)x240(V)	
2	Active Area	mm	72.96(H)x54.72(V)	
3	Screen Size	inch	3.59(Diagonal)	
4	Dot Pitch	mm	0.076(H)x0.228(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	84.55(H) × 65.5(V) × 3.22(T)	Note 3
8	Weight	g	TBD (Typical)	
9	Panel surface treatment	--	Anti-Glare	
10	Display Mode	--	Normally White	

Note 1: Below figure shows dot stripe arrangement.



Note 2: The full color display depends on 8-bit data signal (pin13~36).

Note 3: Not include FPC. Refer next page to get further information.



Outline Dimension of TFT-LCD Module

2. Electrical Specifications

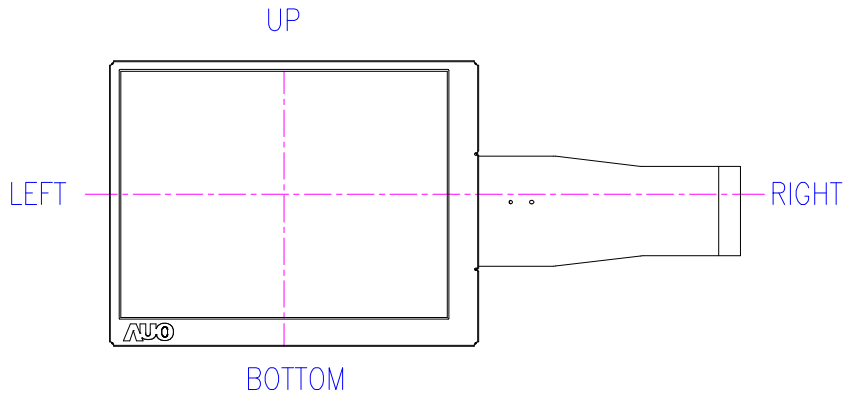
2.1 FPC Pin Assignment

Pin no	Symbol	I/O	Description	Remark
1	AGND	G	Analog ground	
2	AVDD	PS	Analog power	
3	AGND	G	Analog ground	
4	PVDD1	PI	AVDD regulator power	
5	PLL1	I	PLL filter capacitor1	
6	PLL0	I	PLL filter capacitor2	
7	PLLGND	G	PLL ground	
8	GND	G	Digital ground	
9	D0	I	Data input	
10	D1	I	Data input	
11	D2	I	Data input	
12	D3	I	Data input	
13	D4	I	Data input	
14	D5	I	Data input	
15	D6	I	Data input	
16	D7	I	Data input	
17	DCLK	I	Clock	
18	VSYNC	I	Vertical sync input. Negative polarity	
19	HSYNC	I	Horizontal sync input. Negative polarity	
20	SCL	I	Serial communication clock input	
21	SDA	I	Serial communication data input	
22	CSB	I	Serial communication chip select	
23	VCC	I	Digital power	
24	DRV	O	Signal for power transistor of the PVDD boost converter	

25	DRVLED	O	Signal for power transistor of the LED boost converter	
26	LED_ANODE	I	LED power	
27	FBLED	FI	LED boost regulator feedback	
28	GND	G	System ground	
29	FRP	O	Frame polarity	
30	VCAC	PS	VCOM_AC	
31	PVDD2	PI	Charge pump power supply	
32	C1M	C	Connect capacitor for power circuit	
33	C1P	C	Connect capacitor for power circuit	
34	VINT1	PS	Intermediate voltage for charge pump	
35	C3M	C	Connect capacitor for power circuit	
36	C3P	C	Connect capacitor for power circuit	
37	Vgoff_L	PS	Negative power for gate driver output	
38	Vgoff_H	PS	Negative power for gate driver output	Vgoff_L+VCAC
39	VGH	PS	Positive power for gate driver outputs	
40	VCOM	O	VCOM	

I: Digital signal input, O: Digital signal output, G: GND, PI: Power input

C: Power set capacitor connect pin, FI: Feedback input, PS: Power setting,



2.2 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VCC	GND=0	-0.5	5	V	Note 1
	AVDD	AGND=0	-0.5	7	V	Note 1
Operating temperature	Topa	--	0	60	℃	Ambient Temperature
Storage temperature	Tstg	--	-25	80	℃	Ambient Temperature

Note 1: Functional operation should be restricted under normal ambient temperature.

3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

3.1 TFT- LCD Typical Operation Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VCC	2.7	3.3	3.6	V	
		AVDD	5.0	5.25	5.5	V	
		VGH	11.5	12.5	13.5	V	
		VGL		-VGH		V	
Output Signal	H Level	V_{OH}	Vcc-0.4				
	L Level	V_{OL}	GND		GND+0.4		
Input Signal	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by current		I_{st}			200	uA	DCLK is stopped
VCOM		V_{CAC}	4.0	5.6	7.0	Vp-p	AC component
		V_{CDC}		TBD		V	DC component

Note: Above every operation range is based on stable operation from suggested application circuit 3.5.1.

3.2 Register Information

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				DATA											

3.2.1 Register Setting

No.	Description	Address				Initial default value											
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	System setting	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
R1	Timing setting	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	0
R2	Timing setting	0	0	1	0	0	X	X	X	1	0	0	0	0	0	0	0
R3	Timing setting	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
R4	Timing setting	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0	0
R6	Brightness	0	1	1	0	0	X	X	X	1	0	0	0	0	0	0	0
R7	Hue/Saturation	0	1	1	1	0	X	X	X	1	0	0	0	1	0	0	0
R8	VCOM AC/DC	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0
R9	PLL setting	1	0	0	1	0	0	X	X	1	1	0	0	0	0	0	0
R10	DAC setting	1	0	1	0	0	X	X	X	X	X	0	0	0	0	0	0
R11	Contrast/LED	1	0	1	1	0	X	1	0	0	0	0	0	0	1	0	0
R12	Power supply	1	1	0	0	0	X	X	1	0	0	0	0	0	0	0	0

Note 1: “X” is “Don’t care”. “ “ could be modifyed by customer.

Note 2: R5 is totally “Don’t care”.

Register R0

Bit	Function
7	MOD function	**“0” ➔VA,VB,VC are generated by CPH1,CPH2,CPH3(default)** “1” ➔ VA,VB,VC are generated by CPH1.
6	Vertical shift selection	**“0” ➔Scan down.(default)** “1” ➔Scan up.
5	Horizontal shift selection	“0” ➔Shift left. **“1” ➔ Shift right.(default)**
4	Global reset	“0” ➔Chip reset. **“1” ➔Normal operation.(default)**
3	Standby mode	“0” ➔Standby. **“1” ➔ Normal operation.(default)**
2	PVDD DC-DC shutdown	“0” ➔Converter is off. **“1” ➔Converter is on.(default)**
1	LED DC-DC shutdown	**“0” ➔Converter is off.(default)** “1” ➔Converter is on.

0	Charge pump shutdown	"0" ➔Converter is off. **"1" ➔Converter is on.(default)**

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R1

Bit	Function	
10~9	Vertical resolution selection	**"00" ➔ Vertical resolution 240 lines.** "01" ➔ Vertical resolution 234 lines.(default)
8~6	Horizontal resolution selection	**"011" ➔ Horizontal resolution 960 dots.** "110" ➔ Horizontal resolution 1440 dots.(default)
5	Automatic/Manual PAL selection.	"0" ➔PAL/NTSC auto detection disable. **"1" ➔Auto detection enable.(default)**
4	NTSC/PAL selection.	**"0" ➔NTSC input format.(default)** "1" ➔PAL input format.
3~0	Input data format.	**"0XX0" ➔UPS051.(default)** "1000" ➔UPS052 320RGB 24.54MHz. "1001" ➔UPS052 360RGB 27MHz. "1010" ➔YUV mode A 24.54MHz. "1011" ➔YUV mode A 27MHz. "1100" ➔YUV mode B 24.54MHz. "1101" ➔YUV mode B 27MHz. "1110" ➔CCIR656 24.54MHz. "1111" ➔CCIR656 27MHHz.

Note: **Bold blue sentence** is suggested setting for A036QN02 V0. Customer needs to manually set bit 10~6.

Register R2

Bit	Function	
7~0	Horizontal data Start delay selection	"00000000" ➔Ths=Thstyp-128 CLK period. **"10000000" ➔Ths=Thstyp.(default)** "11111111" ➔Ths=Thstyp+127 CLK period.

Note 1: **Bold blue sentence** is suggested setting for A036QN02 V0.

Note 2: Ths: Horizontal data start pulse.

Thstyp: Typical values of horizontal data start pulse.

Register R3

Bit	Function	
10	Gate driver Vgoff setting	"0" ➔Vgoff=Vgoff_L. (default) **"1" ➔ Vgoff switches between Vgoff_L and Vgoff_H.**

9	Dopt function	**"0" ➔R,G,B are sample simultaneous.(default)** "1" ➔R,G,B are sample sequentially.
8~5	Source driver start pulse delay selection.	**"0000" ➔Horizontal start display=Ths.(default)** "1111"➔Horizontal start display=Ths+15 CLK period (default)
4~0	Gate driver start pulse delay selection	"00000" ➔Tstv=Tstvtyp-16 Hsync period **"10000" ➔Tstv=Tstvtyp.(default)** "11111" ➔ Tstv=Tstvtyp+15 Hsync period

Note: **Bold blue sentence** is suggested setting for A036QN02 V0. Customer needs to manually set bit 10.

Register R4

Bit	Function	
10~9	Gate driver start pulse delay selection	**"00" ➔default** "01" ➔Odd frame advance "10" ➔ Even frame advance

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R6

Bit	Function	
7~0	Brightness level adjustment	"00h"➔-128 **"80h"➔0 (default)** "FFh"➔+127

Note 1: Display data=(RGB data) * Contrast +Brightness

Note 2: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R7

Bit	Function	
7~4	YUV Hue color adjustment	"0000"➔-40^0 **"1000"➔0^0 (default)** "1111"➔35^0
3~0	YUV saturation color adjustmenT	"0000"➔0 **"1000"➔1 (default)** "1111"➔1.875

Note 1: C_B=SAT * (C_{B0} * cos(HUE) + C_{R0} * sin(HUE))

C_R=SAT * (C_{R0} * cos(HUE) - C_{B0} * sin(HUE))

Saturation and Hue correction functions are only available for CCIR input format.

Note 2: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R8

Bit	Function	
10~5	VCOM DC level adjustment	"000000"➔0V **"010000"➔0.55V (default)** "110000"➔2.1V
4	VCOM DC Enable function	"0"➔VCOM DC function disabled.VCOM pin is Hi-Z. **"1"➔Enable (default)**
3~0	VCOM AC level adjustment.	"0000"➔4.0V **"1000"➔5.6V (default)** "1111"➔7.0V

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R9

Bit	Function	
10	PLL enable selection	**"0"➔PLL disable (default)** "1"➔PLL enable
7~0	PLL divider selection	"00000000"➔PLL divider -192. **"11000000"➔PLL divider define according horizontal resolution (default)** "11111111"➔PLL divider +63

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R10

Bit	Function	
5	FRP source driver polarity inversion selection.	**"0"➔FRP in phase with the polarity of the DAC output (default)** "1"➔ FRP inverted with respect to the polarity of the DAC output
4~3	Gamma correction selection	**"00"➔Linear Gamma (default)** "01"➔Gamma1. "10"➔Gamma2. "11"➔Gamma3.
2~0	DAC dynamic range adjustment.	**"000"➔1.00V to 4.00V (default)** "001"➔0.89V to 4.11V "010"➔0.77V to 4.23V "011"➔0.66V to 4.34V "100"➔0.54V to 4.46V "101"➔0.43V to 4.57V "110"➔0.31V to 4.69V "111"➔0.20V to 4.80V

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R11

Bit	Function	
9~6	RGB contrast level adjustment	"0000"➔0 **"1000"➔1 (default)** "1111"➔1.875
4~3	DCDC maximum duty cycle selection.	**"00"➔75% (default)** "01"➔80% "10"➔85% "11"➔90%
2~0	DCDC feedback level adjustment	"000"➔0.4V "001"➔0.45V "010"➔0.50V "011"➔0.55V **"100"➔0.60V (default)** "101"➔0.65V "110"➔0.70V "111"➔0.75V

Note: **Bold blue sentence** is suggested setting for A036QN02 V0.

Register R12

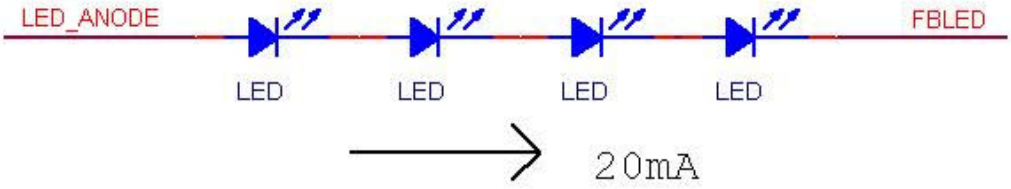
Bit	Function	
8	AVDD power supply external adjustment.	**"0"➔AVDD generated by the internal regulator.** "1"➔AVDD provided by an external regulator (default)

Note: **Bold blue sentence** is suggested setting for A036QN02 V0. Customer needs to manually set bit 8.

3.3 Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	---	20	---	mA	single seral
LED Voltage	V_L	---	13.2	16	V	single seral
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is four LEDs serial type.

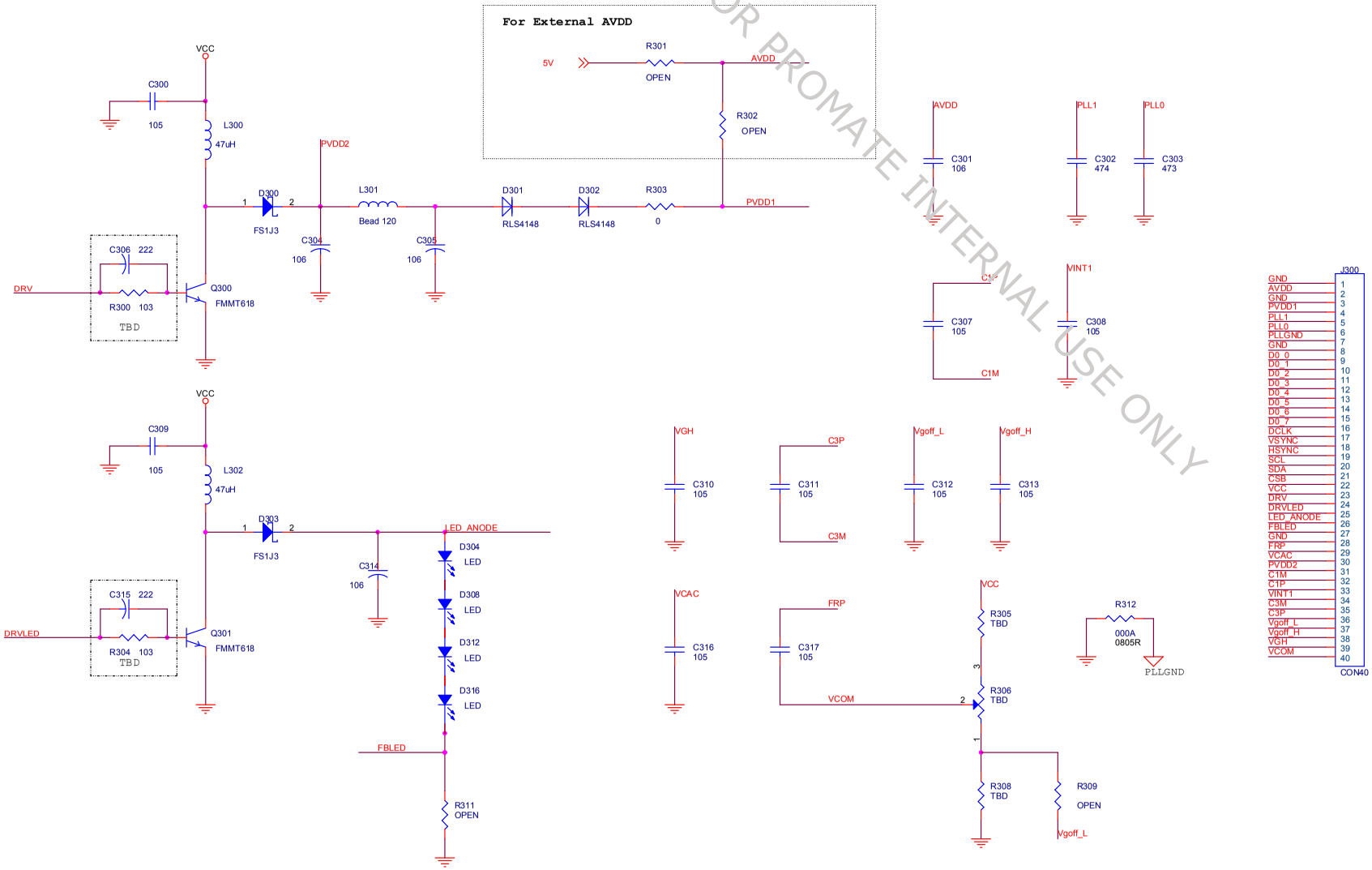


Note 2 :Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED current = 20mA.

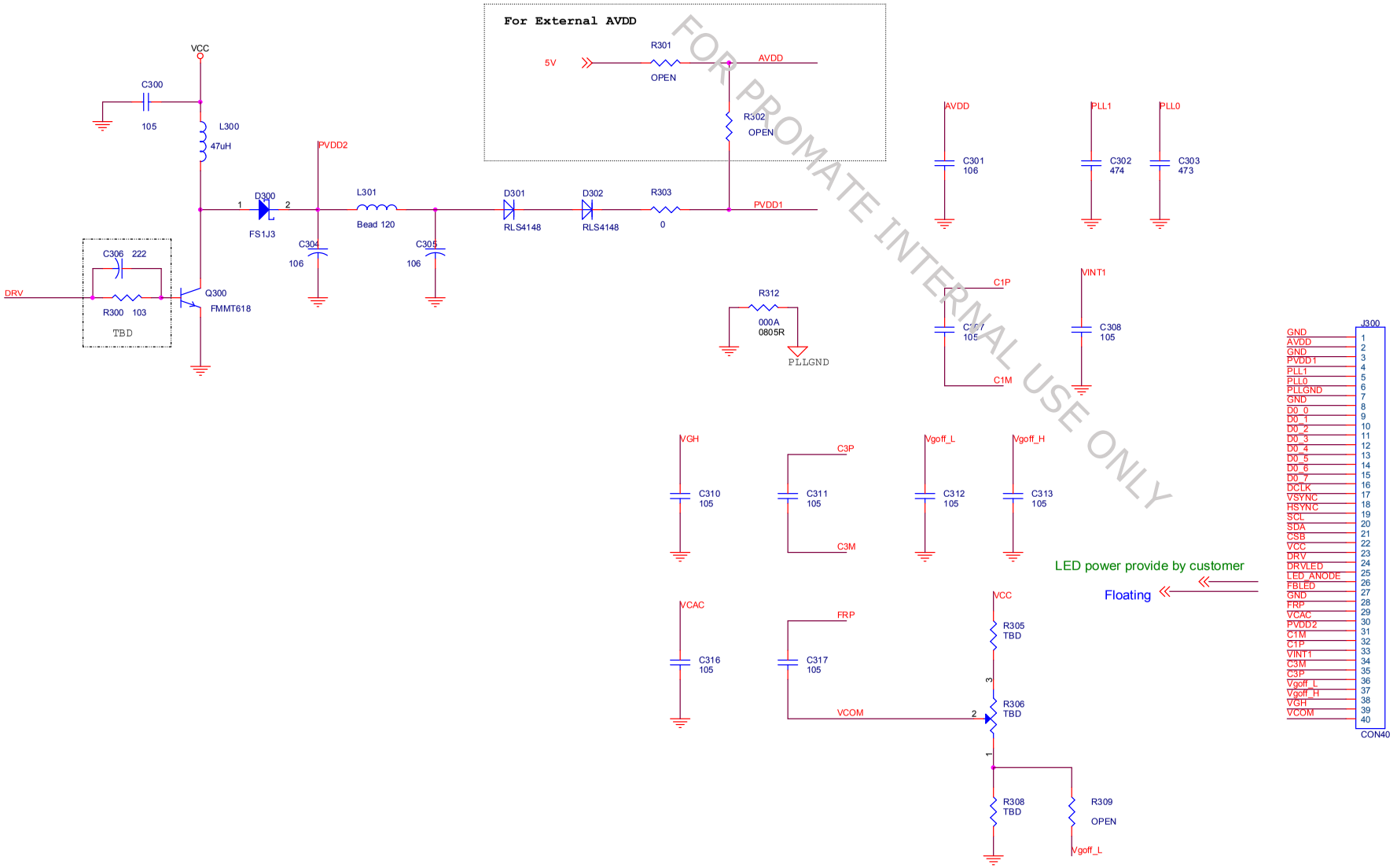
Note 3: If it uses larger LED current I_L more than 20mA, it maybe decreases the LED lifetime.

3.4 Suggested Application Circuit

3.4.1 Suggested Application Circuit



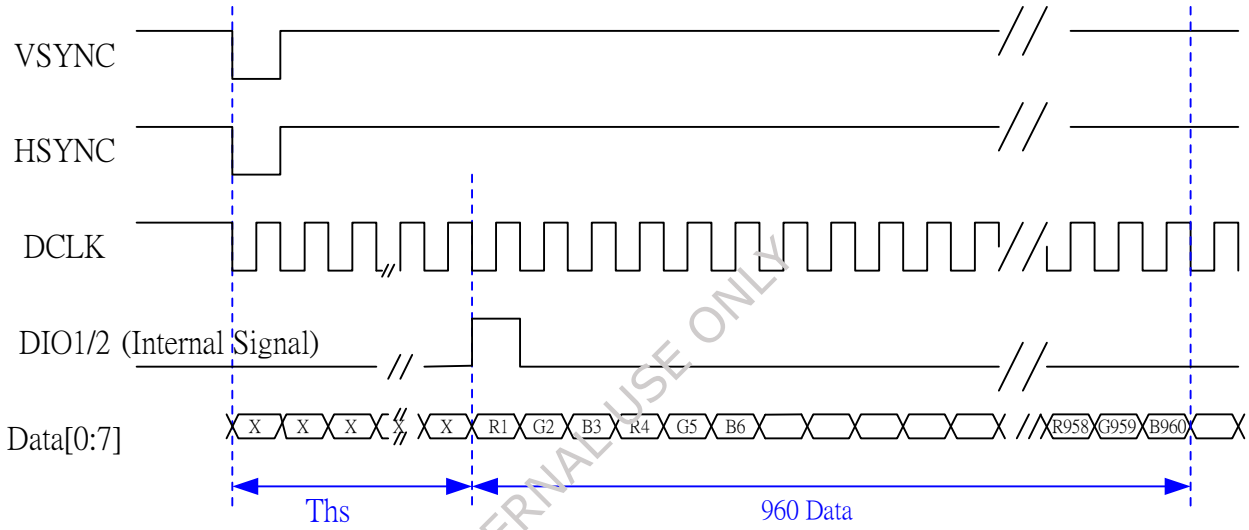
3.4.2 Application Circuit With Using External LED Power Source



3.5 AC Timing

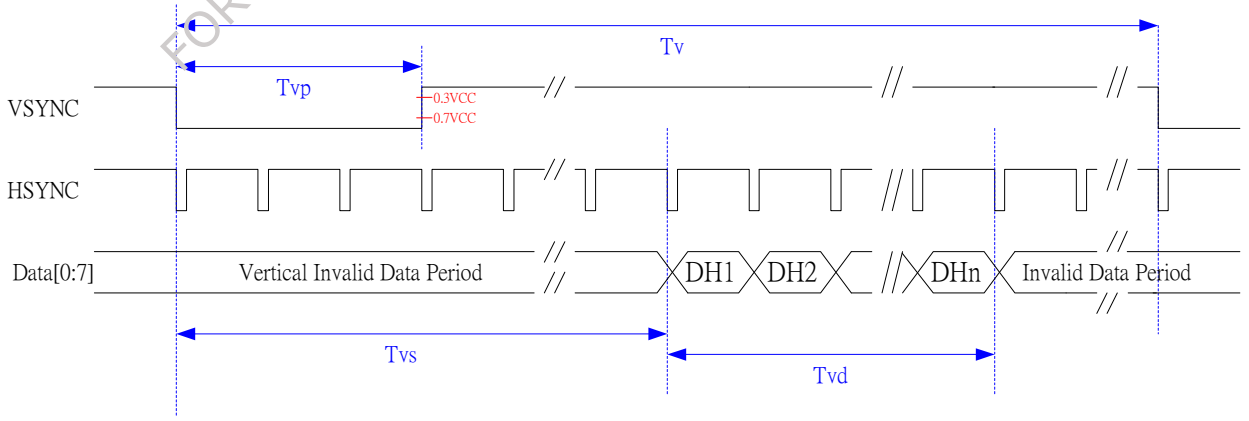
3.5.1 Timing Diagram

3.5.1.1 Relationship of HSYNC, VSYNC, DCLK, and Data



Note 1: DIO1/2 is “internal start pulse” to latch data.

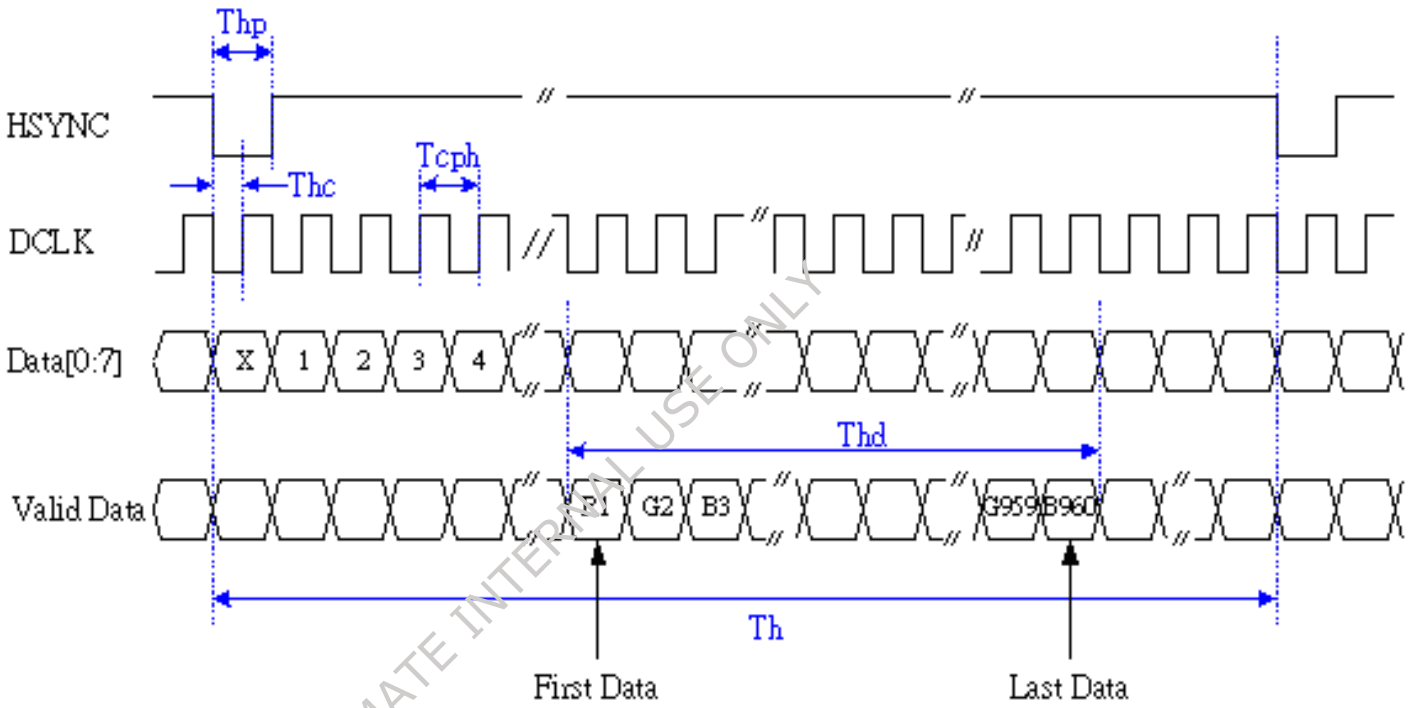
3.5.1.2 Vertical Timing of Input



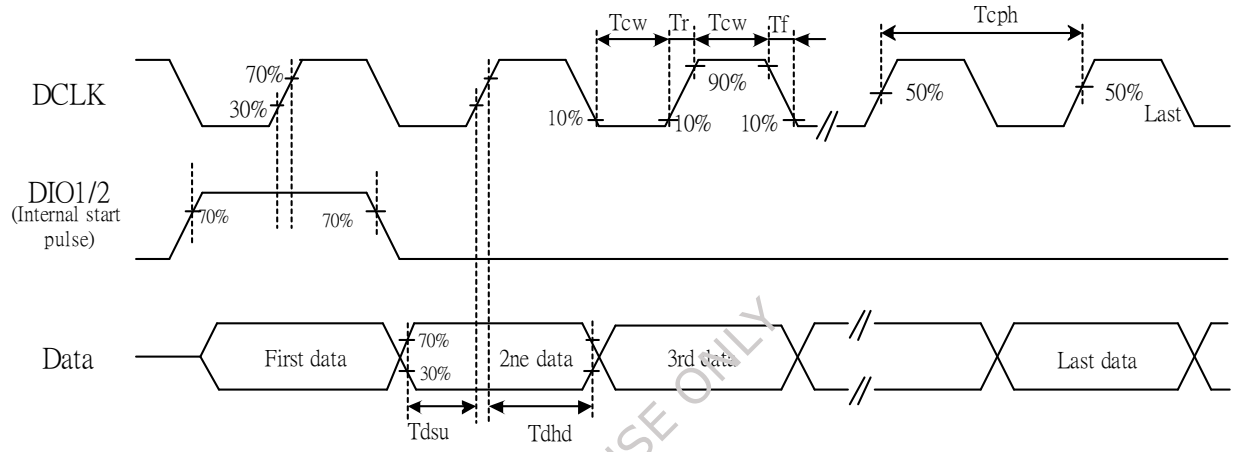
Note : “Tvs” is the blanking area of VSYNC. The fist line is at 14th that will be display on panel.

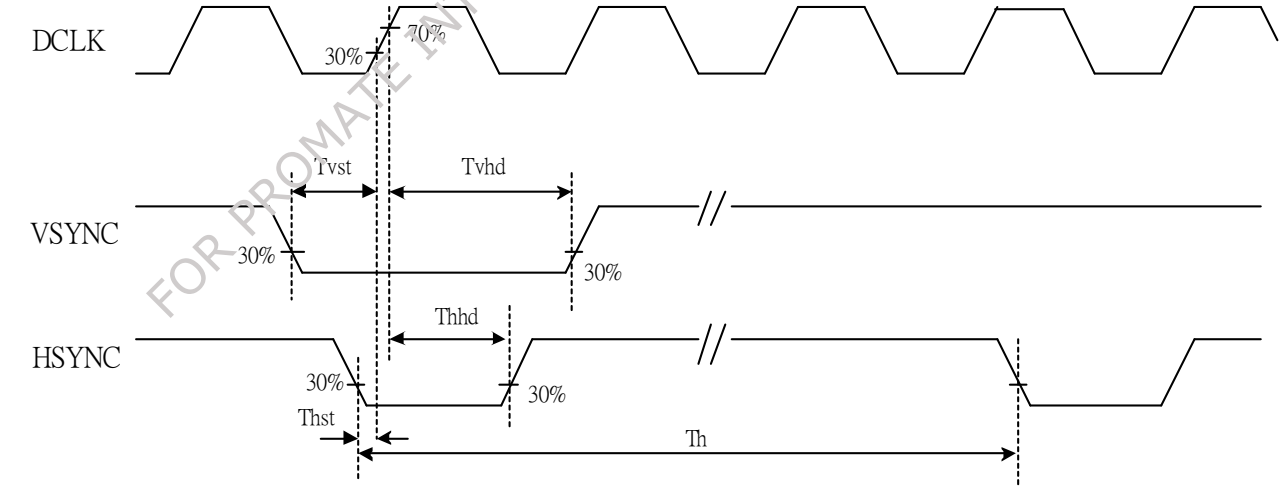
3.5.1.3 Horizontal Timing of Input

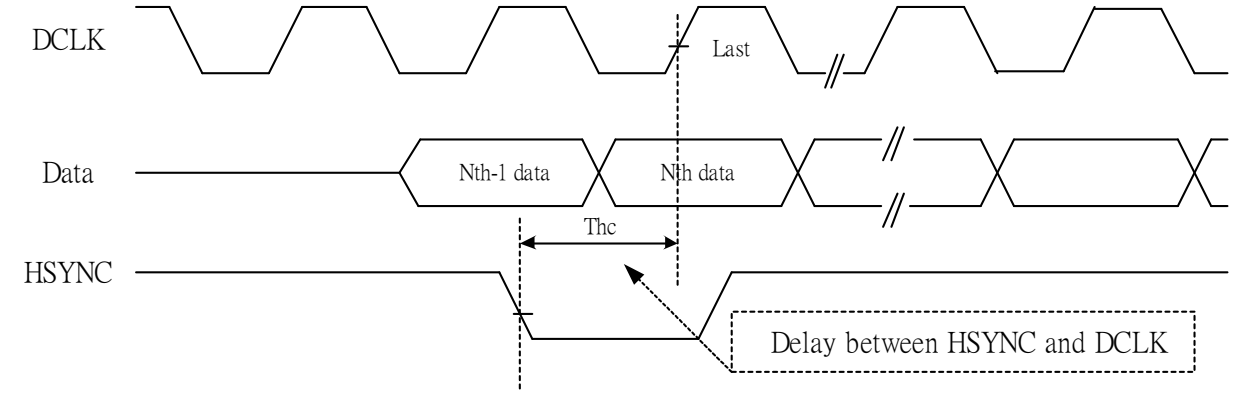
(a)Serial data input



3.5.1.4 Detail Driving Timing







3.5.2 Timing condition

3.5.2.1. Sync Setting

Parameter	Symbol	Min.	Typ.	Max.	Unit.
Clock pulse duty	T_{cw}	40	50	60	%
Delay between Hsync and DCLK	T_{HC}	-	-	1.0	DCLK
Hsync pulse width	Th	60	63.56	67	us
Vsync setup time	Tvst	12	-	-	ns
Vsync hold time	Tvhd	12	-	-	ns
Hsync hold time	Thhd	12	-	-	ns
Data set up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
Vsync to 1st active line	Tvs(NTSC)		17		Hs
	Tvs(PAL)		22		Hs

3.5.2.2 UPS051 Series Input Timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	19.5	-	MHz
DCLK period	Tdclk	-	51.30	-	ns
Hsync period	Th	-	1240	-	DCLK
Active area	Thsapol	-	960	-	DCLK
Delay from Hsync to 1st data input	Ths		181		DCLK

3.5.2.3 UPS051 Parallel Input Timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	6.5	-	MHz
DCLK period	Tdclk	-	154	-	ns
Hsync period	Th	-	413	-	DCLK
Active area	Thsapol	-	320	-	DCLK
Delay from Hsync to 1st data input	Ths		60		DCLK

3.5.2.4 UPS052, YUV input timing:

C.1: 24.54MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	24.54	-	MHz
DCLK period	Tdclk	-	40	-	ns
Delay from Hsync to 1st data input	Ths		252		DCLK

C.2: 27MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	27	-	MHz
DCLK period	Tdclk	-	37	-	ns
Delay from Hsync to 1st data input	Ths		252		DCLK

3.5.2.5 CCIR input timing:

D.1: 24.54MHz NTSC/PAL

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	24.54	-	MHz
DCLK period	Tdclk	-	40	-	ns
Delay from Hsync to 1st data input	Ths		277		DCLK

D.2: 27MHz NTSC

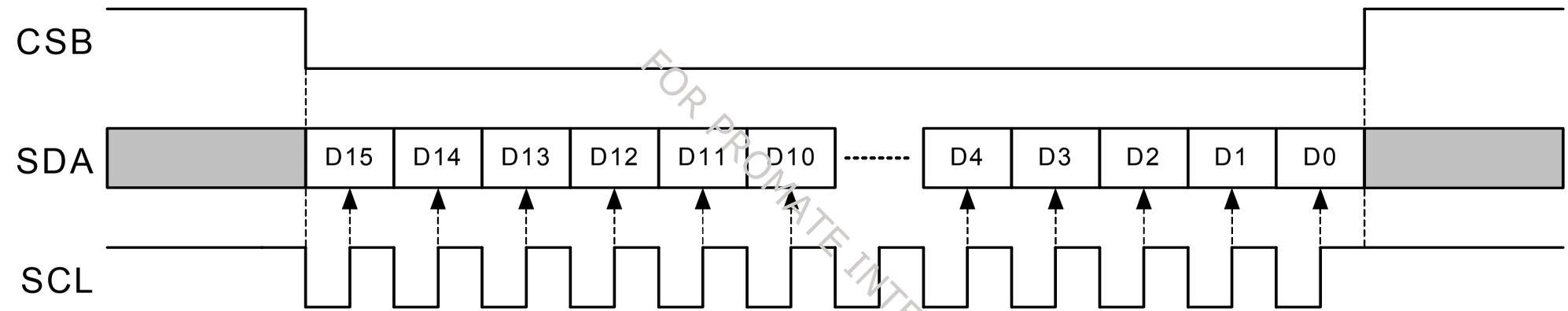
Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	27	-	MHz
DCLK period	Tdclk	-	37	-	ns
Delay from Hsync to 1st data input	Ths		273		DCLK

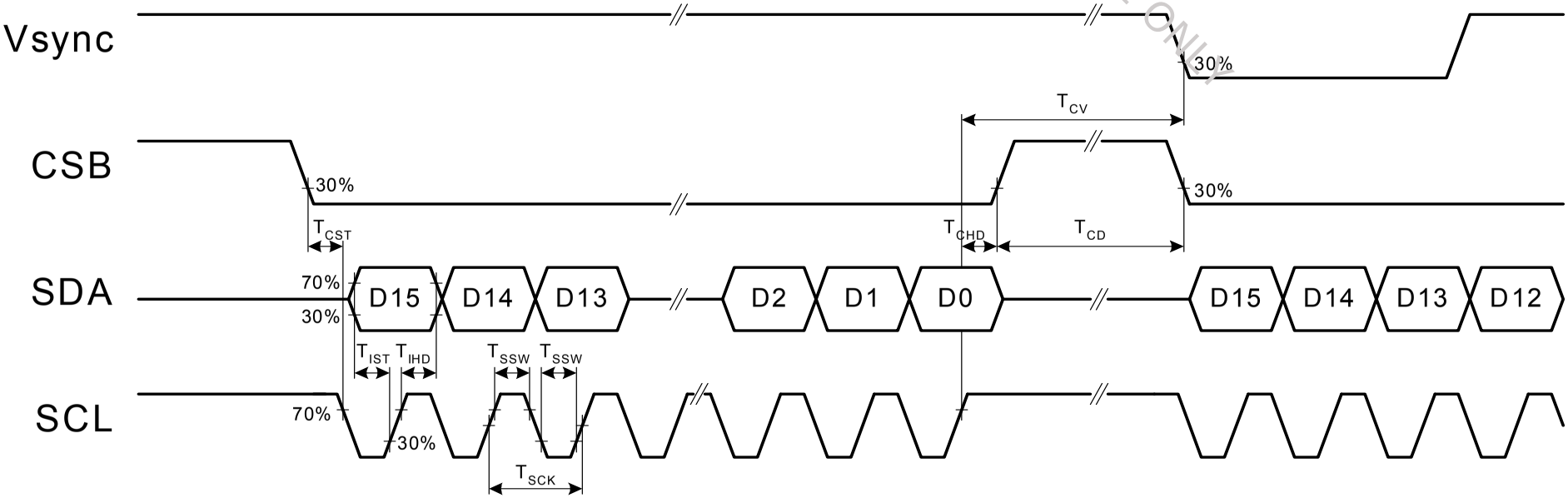
D.3: 27MHz PAL

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fdclk	-	27	-	MHz
DCLK period	Tdclk	-	37	-	ns
Delay from Hsync to 1st data input	Ths		285		DCLK

3.5.2.6 3-wire serial communication AC timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial clock	Tsck	320			ns
SCL pulse duty	Tscw	40	50	60	%
CSB hold time	Tcst	120			ns
Serial data setup time	Tist	120			ns
Serial data hold time	Tiht	120			ns
Serial clock high/low	Tssw	120			ns
Chip select distinguish	Tcd	1			us
CSB to Vsync Time	Tcv	1			us

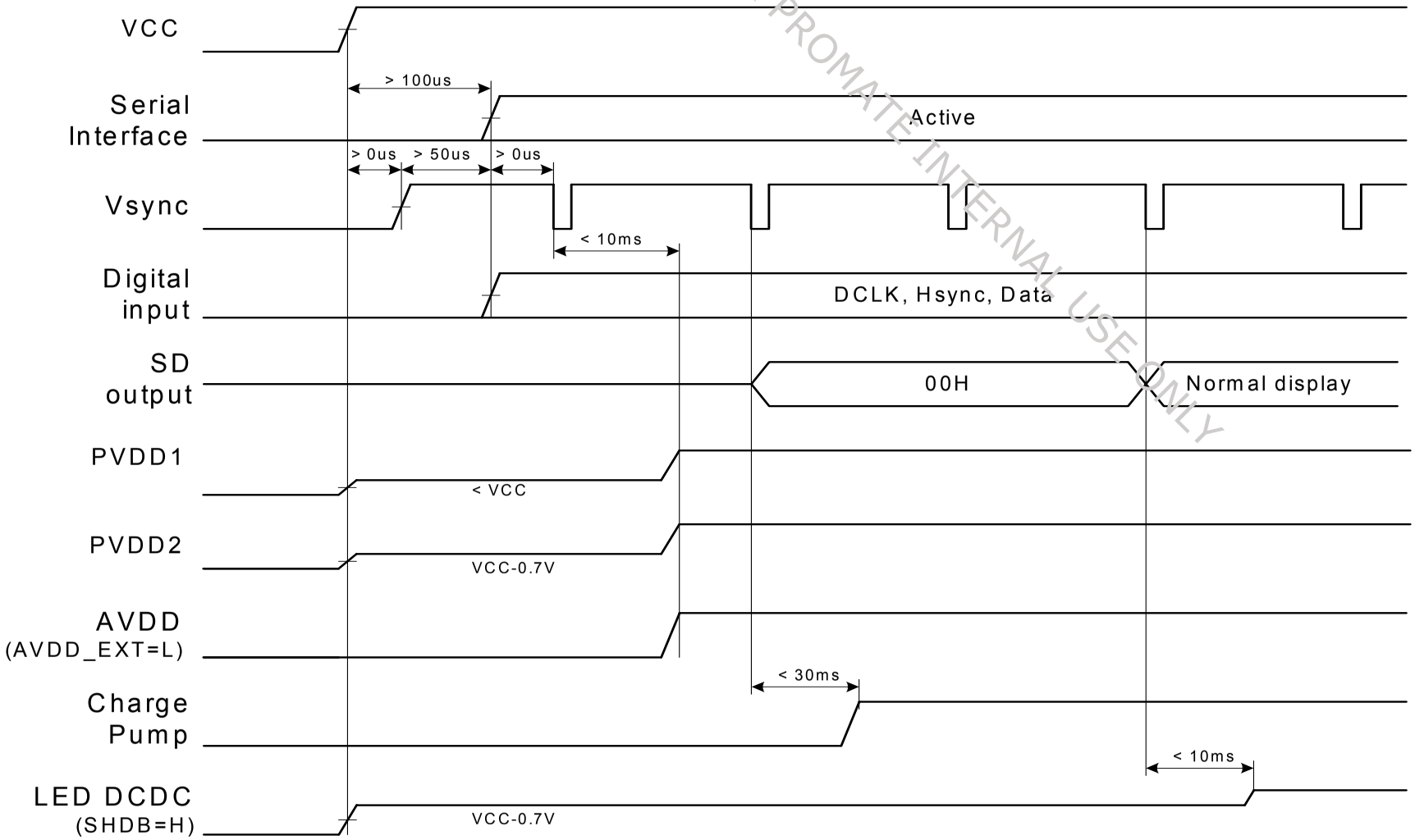




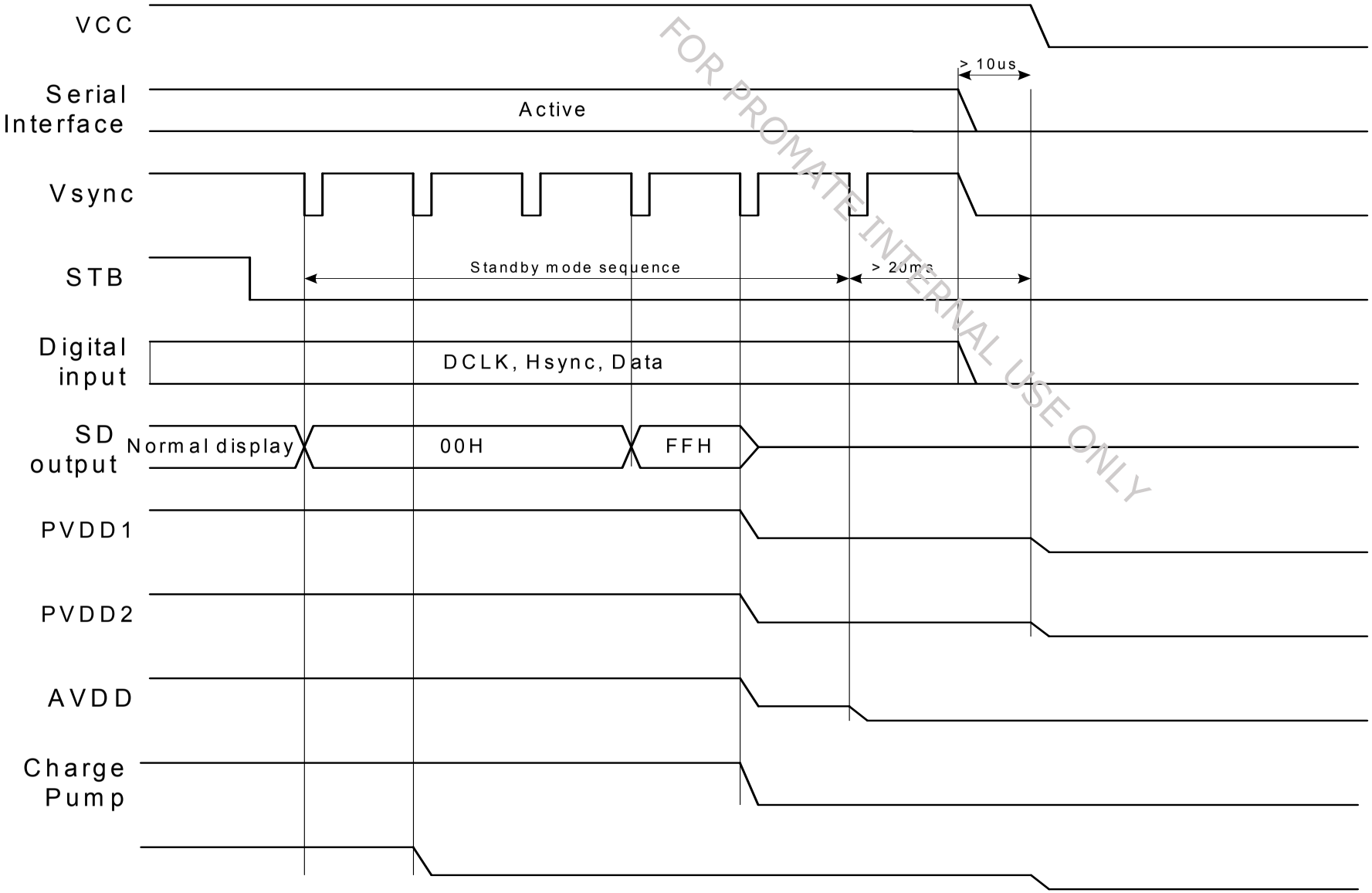
3.6 Power on/off sequence

3.6.1 Internal AVDD

3.6.1.1 Power on sequence

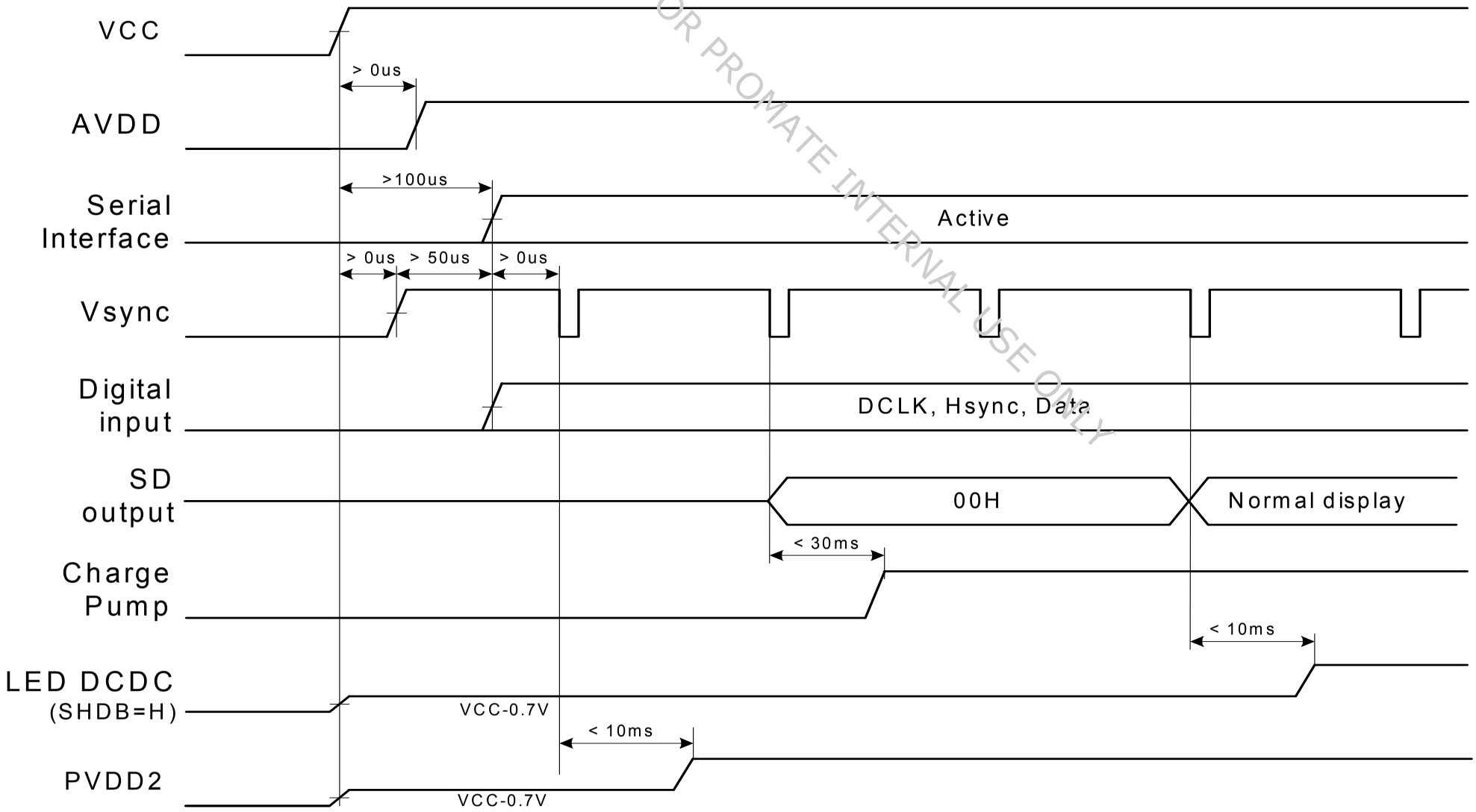


3.6.1.2 Power off sequence

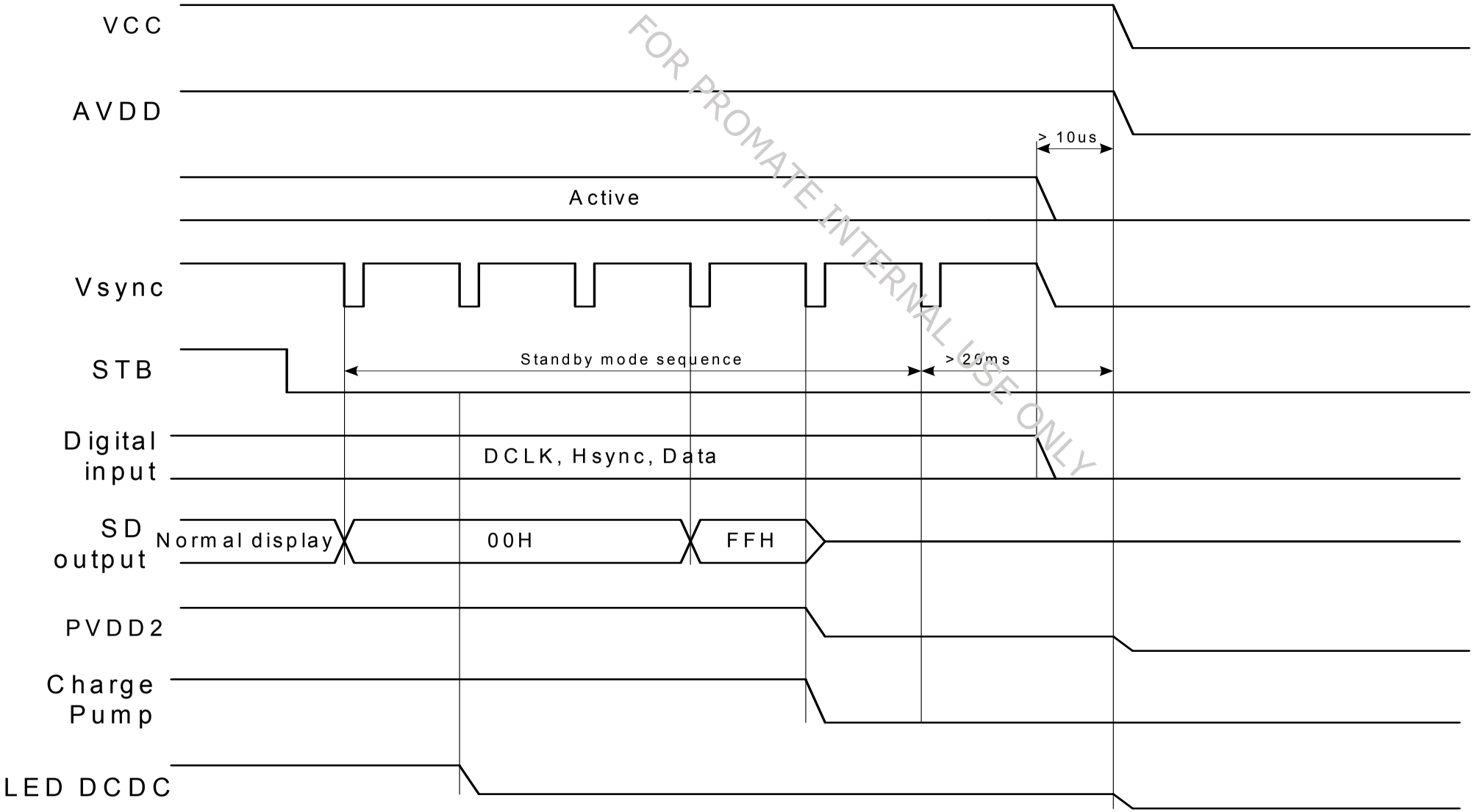


3.6.2 External AVDD

3.6.2.1 Power on sequence



3.6.2.2 Power off sequence



4. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	TBD	30	ms	Note 4
Fall	Tf		-	TBD	60	ms	
Contrast ratio	CR	At optimized viewing	TBD	TBD	-		Note 6, 7
Viewing Angle							
Top			-	40	-		
Bottom		CR≧10	-	60	-	deg.	Note 8
Left			-	60	-		
Right			-	60			
Brightness	Y_L	θ =0°	180	250	-	cd/m^2	Note 9
White Chromaticity	X	θ =0°		TBD			
	y	θ =0°		TBD			

Note 1: Measurement is in the dark room, optical ambient temperature =25℃, and backlight current IL=20 mA

Note 2: To be measured in the dark room.

Note 3:To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

Note 5. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

Note 6. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrastratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 7. White $Vi=V_{i50} + \overline{-}1.5V$

Black $Vi=V_{i50} \pm 2.0V$

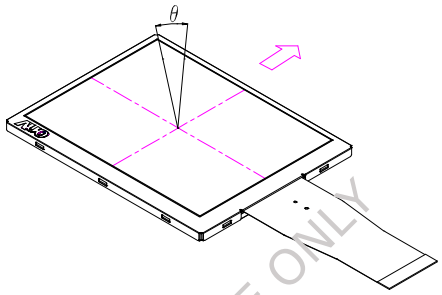
“±” means that the analog input signal swings in phase with COM signal.

“$+\overline{-}$” means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 8. Definition of viewing angle: refer to figure as below.



Note 9. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

5. Absolute Ratings of Ambient Environment

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80℃ 240Hrs	
2	Low Temperature Storage	Ta= -25℃ 240Hrs	
3	High Ttemperature Operation	Ta= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat Shock	-25℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7
10	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient Temperature.

6. Packing Form