

**SPECIFICATION  
FOR  
OLED Module  
BLKD028LEDN019**

MODULE:	
CUSTOMER:	

REV	DESCRIPTION	DATE
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PREPARED BY		
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APPROVED BY		

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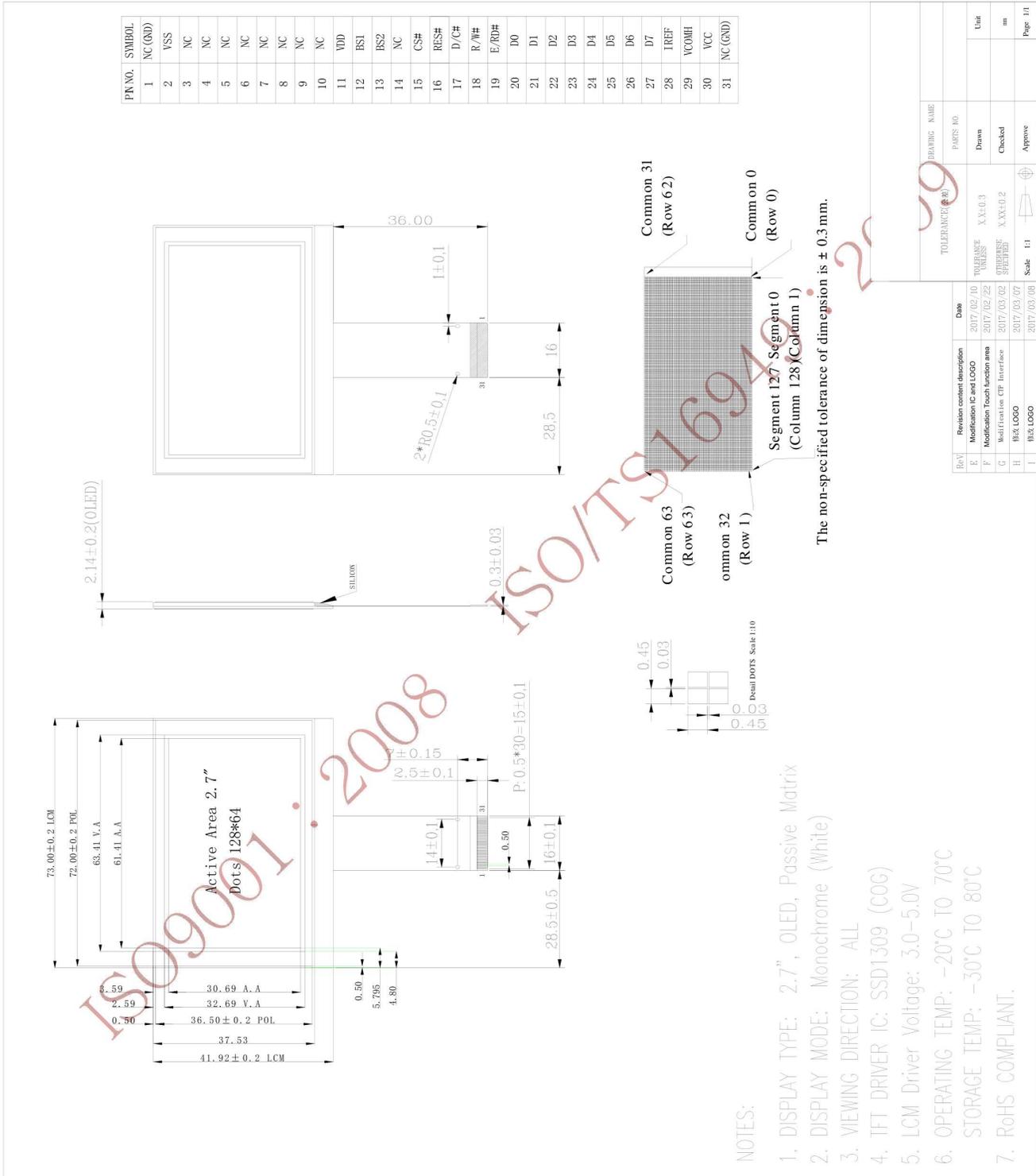
## 1. Basic Specifications

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.41(H) *30.69(V) (2.7inch )	mm	-
Display color	Monochrome (White)	colors	-
Drive Duty	1/64 Duty	-	-
Number of pixels	128*64	dots	-
Pixel pitch	0.48 (H) x 0.48 (V)	mm	-
OLED Controller IC	SSD1309	-	-
Display mode	Passive Matrix	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

### \* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		41.92		mm	-
	Vertical(V)		73.00		mm	-
	Depth(D)		2.14		mm	-
Weight			TBD		g	-

## 2. Outline dimension



### 3. Input terminal Pin Assignment

#### 3.1 OLED

NO.	SYMBOL	DISCRIPTION	I/O															
1	NC.(GND)	No connection.	-															
2	VSS	Ground.	P															
3~10	NC	No connection.	-															
11	VDD	Power Supply pin for core logic operation.	P															
12	BS1	<p>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select</p> <table border="1"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>I2C</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire Serial</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>0</td> <td>1</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		BS1	BS2	I2C	1	0	4-wire Serial	0	0	8-bit 68XX Parallel	0	1	8-bit 80XX Parallel	1	1	I/O
	BS1	BS2																
I2C	1	0																
4-wire Serial	0	0																
8-bit 68XX Parallel	0	1																
8-bit 80XX Parallel	1	1																
13	BS2	<p>Note            (1) 0 is connected to VSS            (2) 1 is connected to VDD</p>																
14	NC	No connection.	-															
15	CS#	This pin is the chip select input connecting to the MCU.	I															
16	RES#	<p>This pin is reset signal input.            When the pin is pulled LOW, initialization of the chip is executed.            Keep this pin pull HIGH during normal operation.</p>	I															
17	D/C#	<p>This pin is Data/Command control pin connecting to the MCU.            When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.            When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.            In I2C mode, this pin acts as SA0 for slave address selection.            When 3-wire serial interface is selected, this pin must be connected to VSS.</p>	I															
18	R/W#	<p>This pin is read / write control input pin connecting to the MCU interface.            When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when</p>	I															

		<p>this pin is pulled HIGH and write mode when LOW.</p> <p>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial or I2C interface is selected, this pin must be connected to VSS.</p>	
19	E/RD#	<p>This pin is MCU interface input.</p> <p>When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.</p> <p>Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.</p> <p>When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial or I2C interface is selected, this pin must be connected to VSS.</p>	I
20~27	D0~D7	<p>These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW.</p> <p>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.</p> <p>When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</p>	I/O
28	IREF	<p>This pin is the segment output current reference pin.</p> <p>IREF is supplied externally.</p>	I
29	VCOMH	<p>COM signal deselected voltage level.</p> <p>A capacitor should be connected between this pin and VSS.</p>	P
30	VCC	<p>Power supply for panel driving voltage. This is also the most positive power voltage supply pin.</p>	P
31	NC(GND)	No connection	-

#### 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	4	V	1,2
Supply Voltage for Display	VCC	0	15	V	1,2
Operating Temperature	TOP	-40	+80	°C	-
Storage Temperature	TSTG	-40	+80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 6 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate

ISO9001 : 2008

ISO/TS16949 : 2009

## 5. Optics & Electrical Characteristics

### 5.1 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VCC	-	2.8	3.0	3.3	V
Supply Voltage for Display	VCC	-	12	13	14	V
High Level Input	VCC	-	0.8xVDD	-	-	V
LOW Level Input	VCC	-	-	-	0.2xVDD	V
High Level Output	VCC	-	0.9xVDD	-	-	V
LOW Level Output	VCC	-	-	-	0.1xVDD	V
50% Check Board operating Current		VCC=13.0	20	22	24	mA

### 5.2 Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
<b>View Angle</b>	(V) $\theta$		160			deg
	(H) $\phi$		160			deg
<b>Contrast Ratio</b>	CR	Dark	2000:1		—	—
<b>Response Time</b>	T rise	—		10		$\mu$ s
	T fall	—		10		$\mu$ s
<b>Display with 50% check Board Brightness</b>			60	80		cd/m <sup>2</sup>
<b>CIE x (Yellow)</b>		(CIE1931)	0.45	0.47	0.49	
<b>CIE y (Yellow)</b>		(CIE1931)	0.48	0.50	0.52	

## 6. AC Characteristics

### Conditions:

Voltage referenced to  $V_{SS}$

$V_{DD}=1.65$  to  $3.3V$

$T_A = 25^{\circ}C$

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$F_{OSC}^{(1)}$	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.8V$	360	450	540	kHz
$F_{FRM}$	Frame Frequency	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	$F_{OSC} \times 1/(D \times K \times 64)$ <sup>(2)</sup>	-	Hz
RES#	Reset low pulse width		3	-	-	$\mu s$

### Note

<sup>(1)</sup>  $F_{OSC}$  stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

<sup>(2)</sup> D: divide ratio (default value = 1)

K: number of display clocks per row period (default value = 69)

Please refer to 9.5 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

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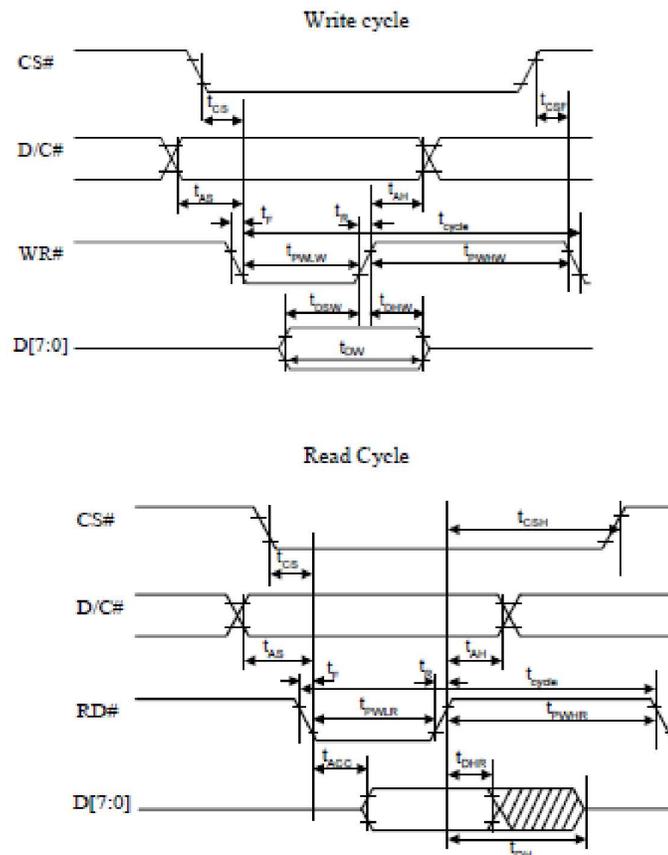


## 6.2 8080-Series MPU Parallel Interface Timing Characteristics:

( $V_{DD} - V_{SS} = 1.65V \sim 3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	20	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DW}$	Data Write Time	70	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLr}$	Read Low Time	120	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHr}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_r$	Rise Time	-	-	40	ns
$t_f$	Fall Time	-	-	40	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics

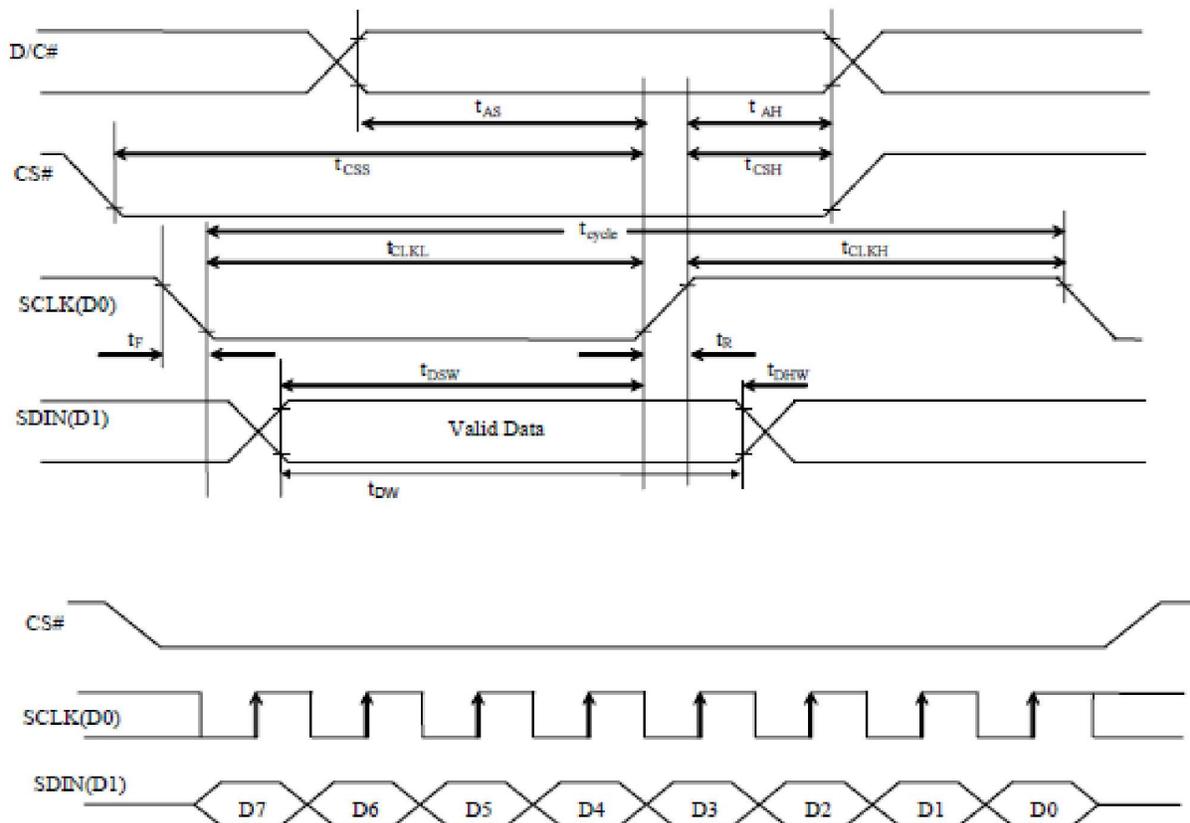


### 6.3 Serial Interface Timing Characteristics: (4-wire Serial)

( $V_{DD} - V_{SS} = 1.65V \sim 3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	50	-	-	ns
$t_{DW}$	Data Write Time	55	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{CLKL}$	Clock Low Time	50	-	-	ns
$t_{CLKH}$	Clock High Time	50	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

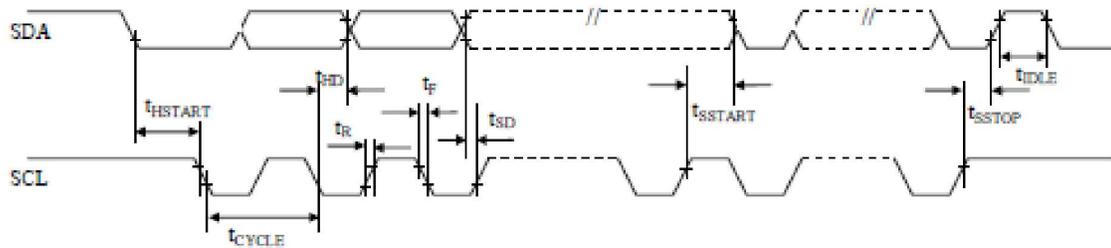
Figure 13-3 : Serial interface characteristics (4-wire SPI)



## 6.4 IIC Interface

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	2.5	-	-	us
$t_{\text{HSTART}}$	Start condition Hold Time	0.6	-	-	us
$t_{\text{HD}}$	Data Hold Time (for "SDA <sub>OUT</sub> " pin)	0	-	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " pin)	300	-	-	ns
$t_{\text{SD}}$	Data Setup Time	100	-	-	ns
$t_{\text{SSTART}}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
$t_{\text{SSTOP}}$	Stop condition Setup Time	0.6	-	-	us
$t_{\text{r}}$	Rise Time for data and clock pin	-	-	300	ns
$t_{\text{f}}$	Fall Time for data and clock pin	-	-	300	ns
$t_{\text{IDLE}}$	Idle Time before a new transmission can start	1.3	-	-	us

Figure 13-5 : I<sup>2</sup>C interface Timing characteristics



ISO9001 : ✓

## 7. Appearance Inspection

### 7.1 Appearance Condition

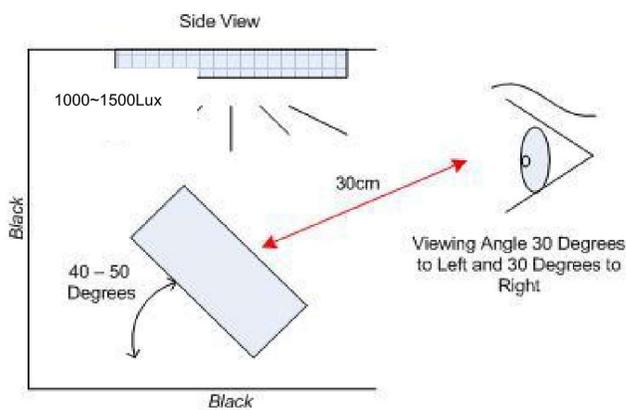
9.1.1 Environment:  $22 \pm 3^{\circ}\text{C}$ , Inspection distance :  $30 \pm 5\text{cm}$ .

9.1.2 Rotation angle :  $\pm 45^{\circ}$

9.1.3 Lighting illumination : 1000~1200Lux

9.1.4 Background : Black

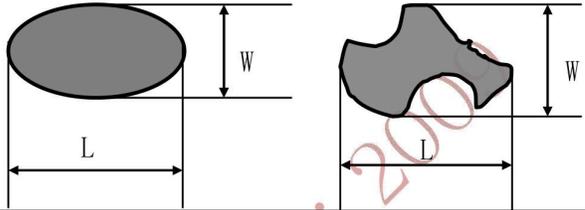
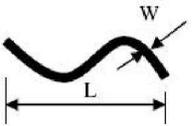
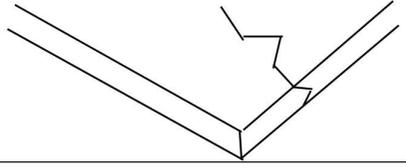
9.1.5 Inspection time : 30s each piece



Remark:

Inspection criteria are valid for the complete Module (TP + OLED) including reverse Printing and Logo printing

## 7.2 Appearance Criterion

No.	Item	Criteria for defects (Unit: mm)
1	Dot Defects (Particle/Dirt/ Dent/Bubble)	1、 $D \leq 0.2$ mm; Ignore
		2、 $0.2 \text{ mm} < D \leq 0.5 \text{ mm}$ , $N \leq 5$ , Distance $\geq 70$ mm $D \geq 5$ mm is not allowed. $D = \frac{(W + L)}{2}$
		
2	Line type Defects (Scratch/Dirt/Particle)	1、 $W \leq 0.063$ mm , Ignore
		2、 $0.063 \text{ mm} < W \leq 0.1 \text{ mm}$ , $L \leq 8$ mm (length in total), $N \leq 4$ ; Distance $\geq 70$ mm Other is not allowed.
		
3	Edge Chipping	Allow: Edge Chips/chamfered Edges: Corner: $D \leq 0.3$ mm Polished edges: $D \leq 0.25$ mm, Ignore; $0.25 \text{ mm} < D \leq 0.4 \text{ mm}$ , $N \leq 5$ per edge allowed Heat marks on polished edged: Width max. 0.15mm, length max.4.0mm. Max.2 per 500mm, min. distance >40mm
4	Glass Crack	Crack is potential to enlarge, any type is not allowed. 
5	No visible color change when compared with the approved sample	
Remark	For No.1.2 and 2.2 8 defects in total are allowed A concentration of defects is not allowed, definition in accordance with DIN ISO 10110-7	

## 8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30℃,30 min ↔ 80℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

## 9. Cautions and Handling Precautions

### 9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

### 9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

## 10. Packing

---TBD-----

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