SPECIFICATION
FOR
OLED Module
BLKD072LEDN001-C001B

MODULE:	
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2016.10.19

	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2016.10.19	V1.0	ALL	FIRST ISSUE

Contents

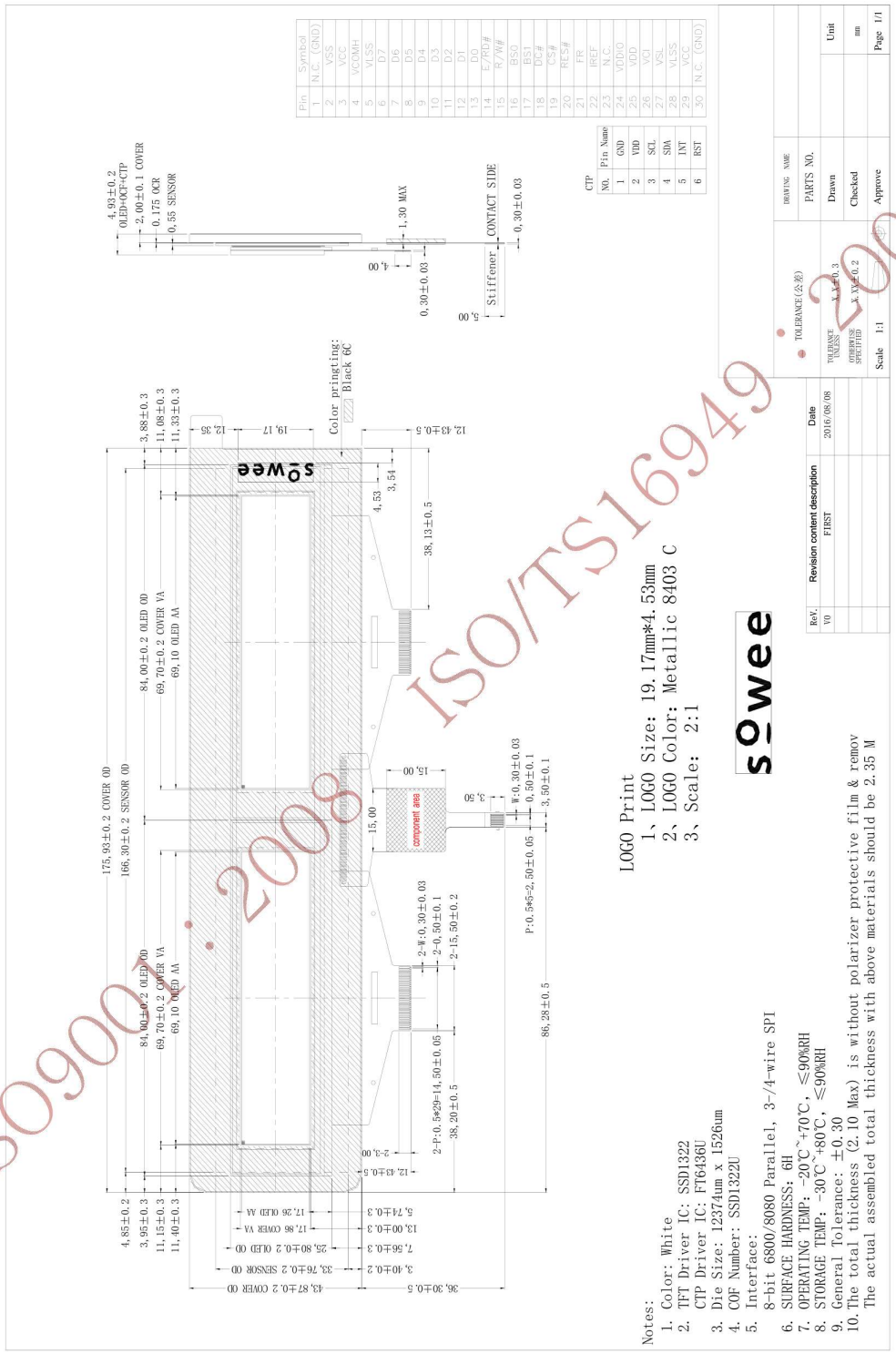
1. Basic Specifications

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	69.10(H) *17.26(V) (2.8inch)	mm	-
CTP View area	69.70(H)*17.86(V)	mm	
Display color	Monochrome with 16 Gray Scales (White)	colors	-
Drive Duty	1/64 Duty	-	-
Number of pixels	256(RGB)*64	dots	-
Pixel pitch	0.27 (H) x 0.27 (V)	mm	-
OLED Controller IC	SSD1322	-	-
CTP Driver IC	FT6436U		
Display mode	Passive Matrix	-	-
Touch mode	Single point and Gestures		
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		175.93		mm	-
	Vertical(V)		43.87		mm	-
	Depth(D)		4.93		mm	-
Weight			TBD		g	-

2. Outline dimension



3. Input terminal Pin Assignment

3.1 OLED

NO.	SYMBOL	DISCRIPTION	I/O
1	NC.(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.	
2	VSS	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground	P
3	VCC	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.	P
4	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.	P
5	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.	P
6-13	D7~D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.	I/O
14	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.	I

<table>
<tr><td>15</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input.
Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>16</td><td>BS0</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:<table><tr><th></th><th>BS0</th><th>BS1</th></tr><tr><td>3-wire Serial</td><td>1</td><td>0</td></tr><tr><td>4-wire Serial</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr></table></td><td rowspan="2">I</td></tr>
<tr><td>17</td><td>BS1</td></tr>
<tr><td>18</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register.
When 3-wire serial mode is selected, this pin must be connected to VSS.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td><td>I</td></tr>
<tr><td>19</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only
when CS# is pulled low.</td><td>I</td></tr>
<tr><td>20</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td><td>I</td></tr>
<tr><td>21</td><td>FR</td><td>Frame Frequency Triggering Signal
This pin will send out a signal that could be used to identify the driver</td><td>O</td></tr>
</table>

		status. Nothing should be connected to this pin. It should be left open individually.	
22	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10μA maximum.	I
23	N.C.	NC	
24	VDDIO	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.	P
25	VDD	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.	P
26	VCI	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.	P
27	VSL	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.	P
28	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.	P
29	VCC	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.	P
30	N.C. (GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the	

		function pins. These pins must be connected to external ground as the ESD protection circuit.	

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDD	Supply voltage.	P
3	SCL	I2C clock input.	I
4	SDA	I2C data input and output	I
5	INT	External interrupt to the host.	I
6	RST	External Reset, Low is active.	I

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	60	mA	1, 2
Operating Temperature	T_{OP}	-40	85	℃	3
Storage Temperature	T_{STG}	-40	90	℃	3
Life Time (100 cd/m^2)		15,000	-	hour	4
Life Time (80 cd/m^2)		25,000	-	hour	4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC = 12.0V, Ta = 25°C, 50% Checkerboard.
Software configuration follows Section 4.5 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions

5. Optics & Electrical Characteristics

5.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 12.0V.
Software configuration follows Section 4.5 Initialization.

5.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	
Supply Voltage for Display	V_{CC}	Note 5	11.5	12.0	12.5	
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100μA	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100μA	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	180	300	μA
Operating Current for V_{CC}	I_{CC}	Note 6		15.6	19.5	mA
		Note 7	-	26.1	32.7	mA
		Note 8	-	44.7	55.9	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	20	100	μA
Sleep Mode Current for V_{DDIO}	$I_{DDIO, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{CI} = 2.8V, V_{CC} = 12.0V, 30% Display Area Turn on.
Note 7: V_{CI} = 2.8V, V_{CC} = 12.0V, 50% Display Area Turn on.
Note 8: V_{CI} = 2.8V, V_{CC} = 12.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

5.3 AC Characteristics

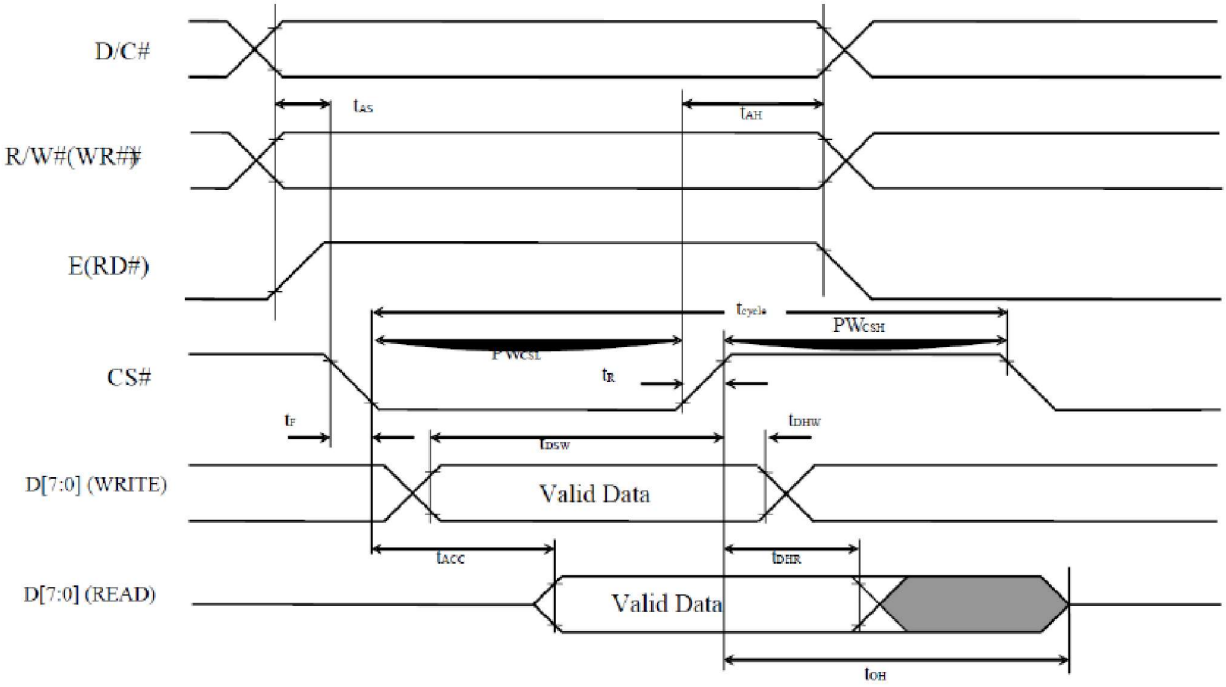
5.3.1 6800-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	450	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 1.65V-2.1V, VCI - VSS = 2.4V-3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	150	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 2.1V-VCI , VCI - VSS = 2.4V-3.5V, TA = 25°C)



5.3.2 8080-Series MPU Parallel Interface Timing Characteristics:

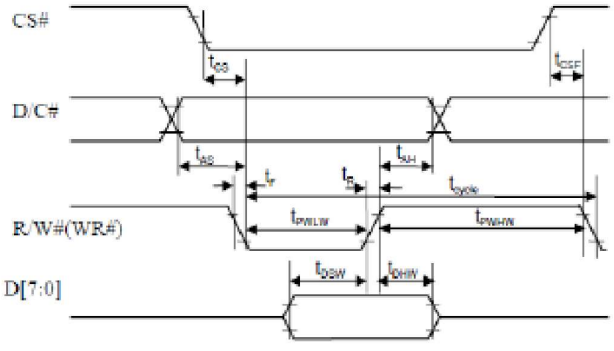
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	220	ns
t_{PWLR}	Read Low Time	200	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 1.65V-2.1V, VCI - VSS = 2.4V-3.5V, TA = 25°C)

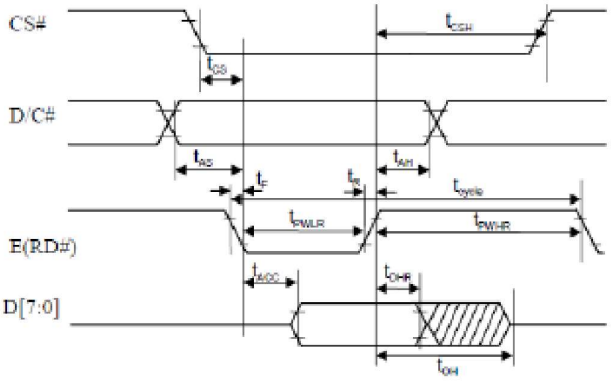
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 2.1V-VCI , VCI - VSS = 2.4V-3.5V, TA = 25°C)

Write cycle



Read cycle



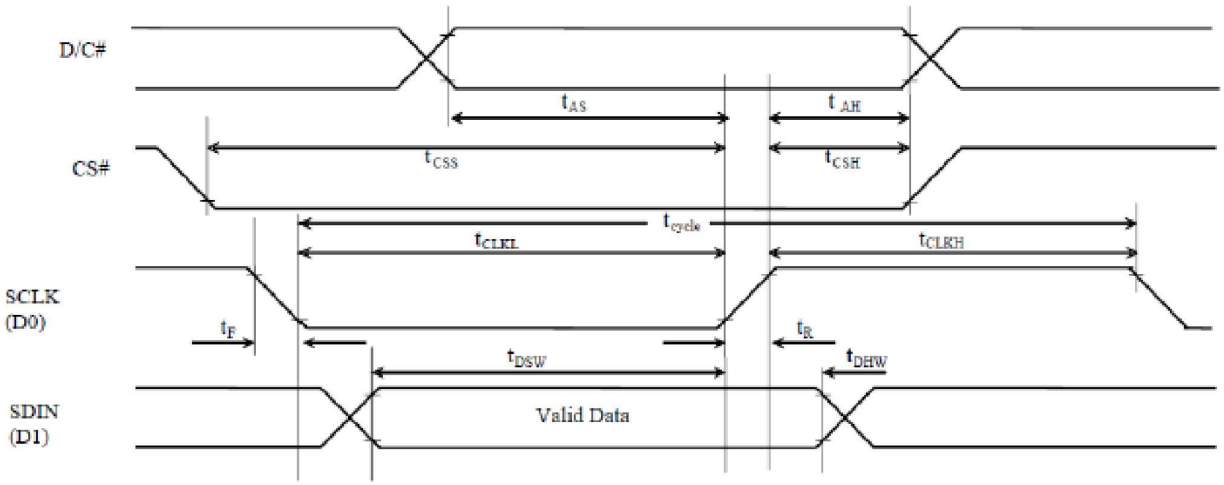
5.3.3 Serial Interface Timing Characteristics: (4-wire Serial)

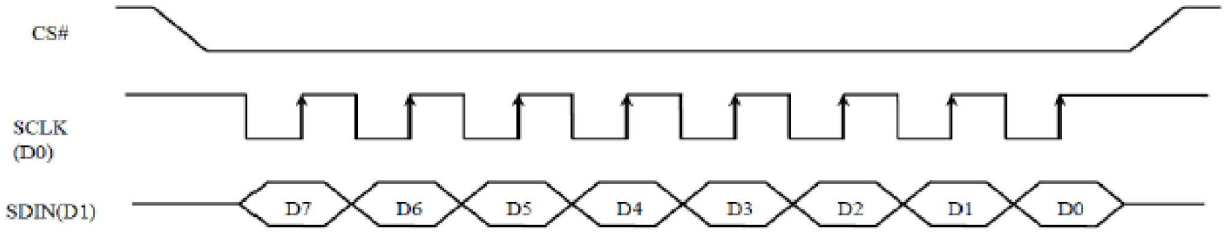
Symbol	Description	Min	Max	Unit
t_{cyde}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	35	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	40	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 1.65V-2.1V, VCI - VSS = 2.4V-3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_{cyde}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	35	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	40	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 2.1V-VCI , VCI - VSS = 2.4V-3.5V, TA = 25°C)





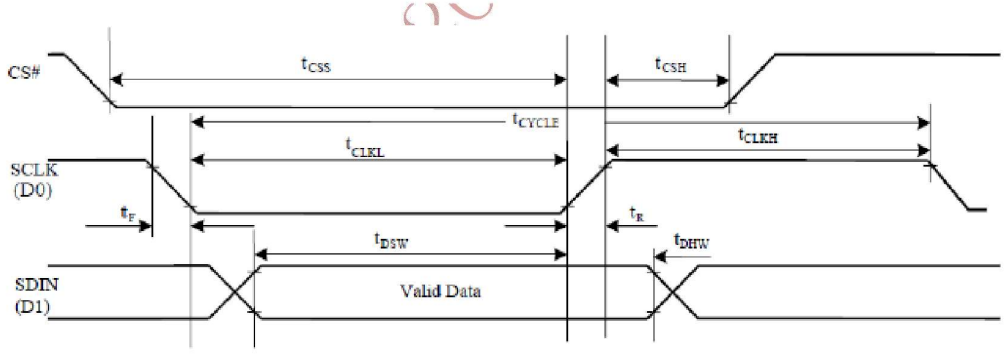
5.3.4 Serial Interface Timing Characteristics: (3-wire Serial)

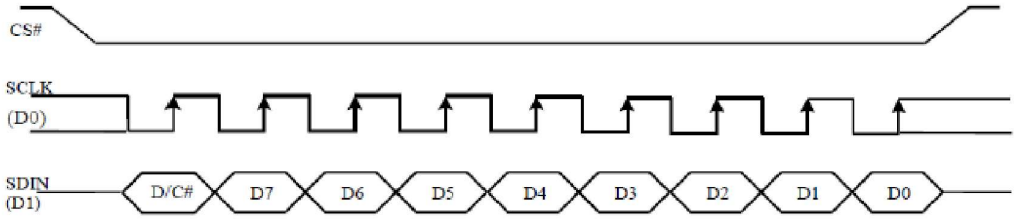
Symbol	Description	Min	Max	Unit
t_{cyde}	Clock Cycle Time	300	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	35	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	25	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 1.65V-2.1V, VCI - VSS = 2.4V-3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_{cyde}	Clock Cycle Time	300	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	25	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	25	-	ns
t_{CLKH}	Clock High Time	25	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDDIO -VSS = 2.1V-VCI , VCI - VSS = 2.4V-3.5V, TA = 25°C)





6. Functional Specification

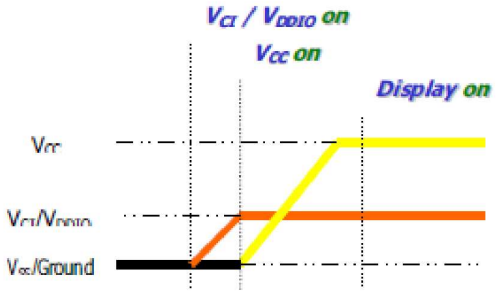
Refer to the Technical Manual for the SSD1322

6.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

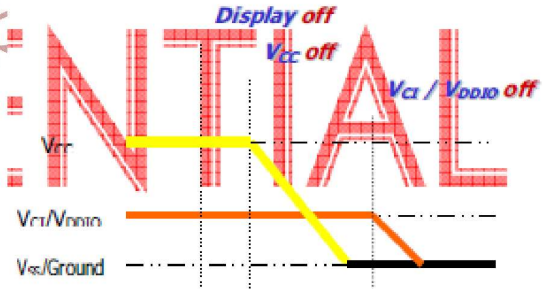
6.1.1 Power up Sequence:

1. Power up VCI / VDDIO
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 200ms
   (When VCC is stable)
7. Send Display on command



6.1.2 Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms
   (When VCC is reach 0 and panel is completely discharges)
4. Power down VCI / VDDIO



Note 9:

1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC inside the driver IC, VCC becomes lower than VCI whenever VDD, VDDIO is ON and VCC is OFF.

2) VCC should be kept float (disable) when it is OFF.

3) Power Pins (VDD, VDDIO, VCC) can never be pulled to ground under any circumstance.

4) VCI, VDDIO should not be power down before VCC power down.

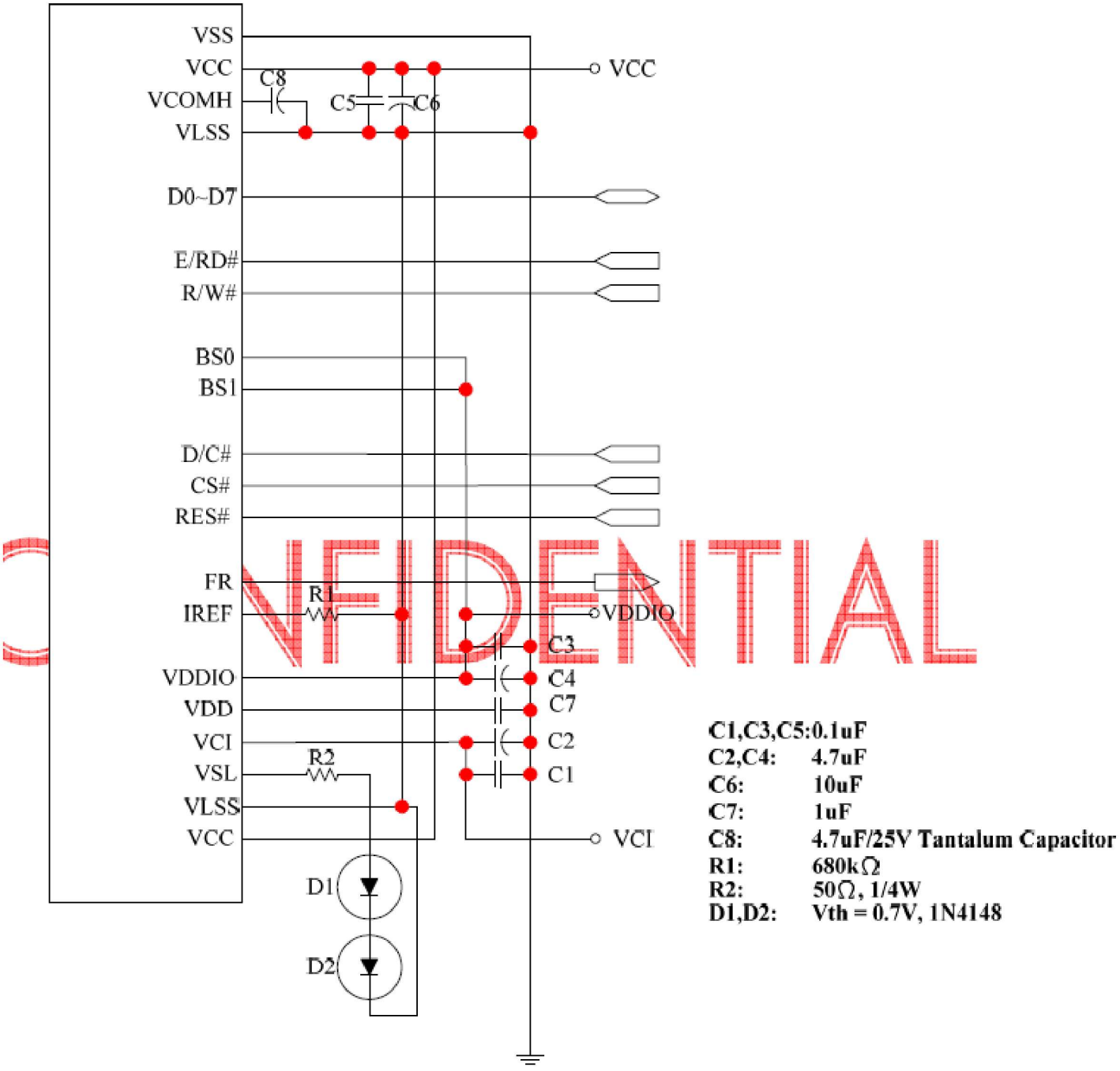
6.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 480×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 7Fh

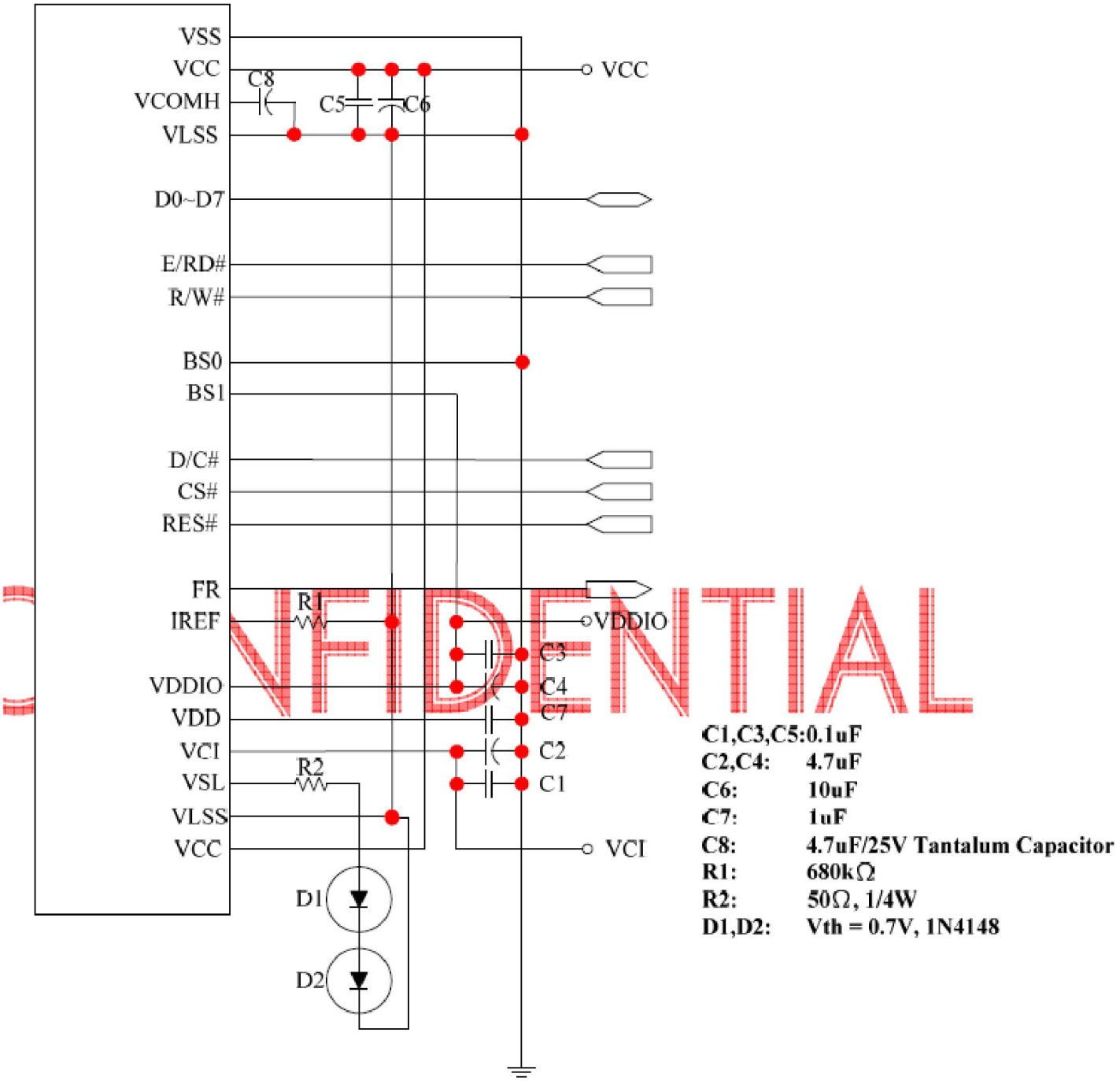
6.3 Application circuit

6.3.1 6800-Series MPU Parallel Interface and VCC Supplied Externally



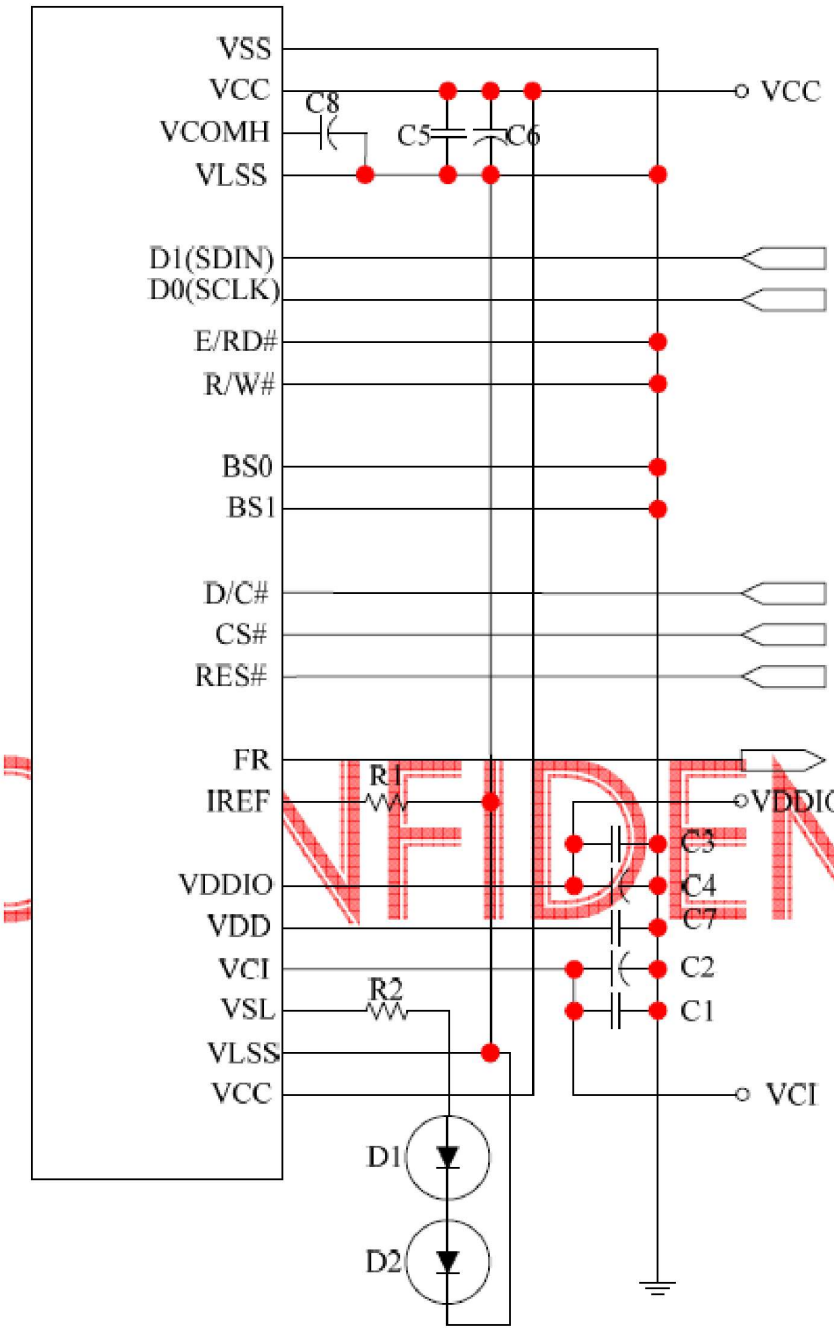
C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680kΩ
R2: 50Ω, 1/4W
D1,D2: Vth = 0.7V, 1N4148

6.3.2 8080-Series MPU Parallel Interface and VCC Supplied Externally



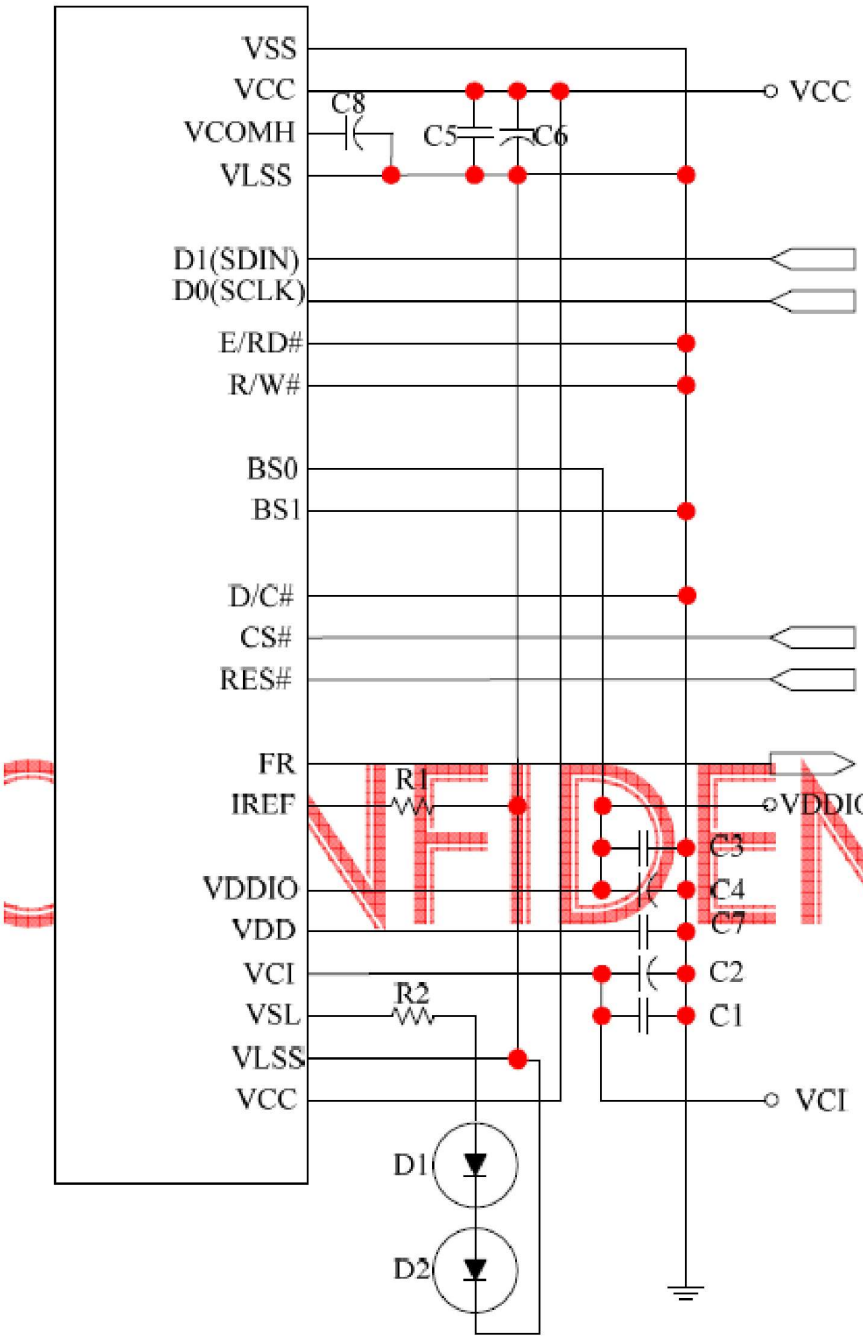
C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680kΩ
R2: 50Ω, 1/4W
D1,D2: Vth = 0.7V, 1N4148

6.3.3 4wire SPI and VCC Supplied Externally



C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680kΩ
R2: 50Ω, 1/4W
D1,D2: Vth = 0.7V, 1N4148

6.3.4 3wire SPI and VCC Supplied Externally



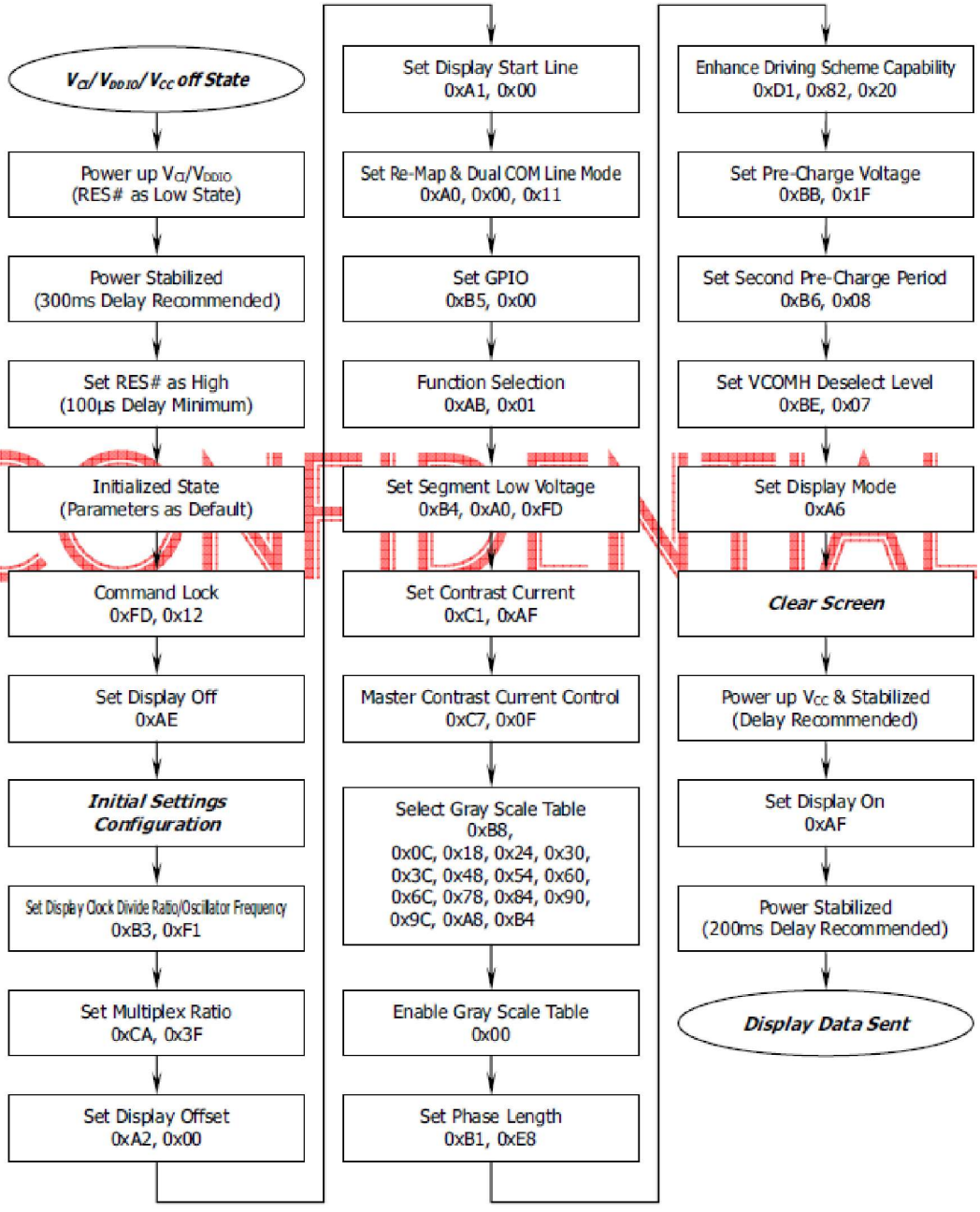
C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680kΩ
R2: 50Ω, 1/4W
D1,D2: Vth = 0.7V, 1N4148

7. Actual Application Example

Command usage and explanation of an actual example

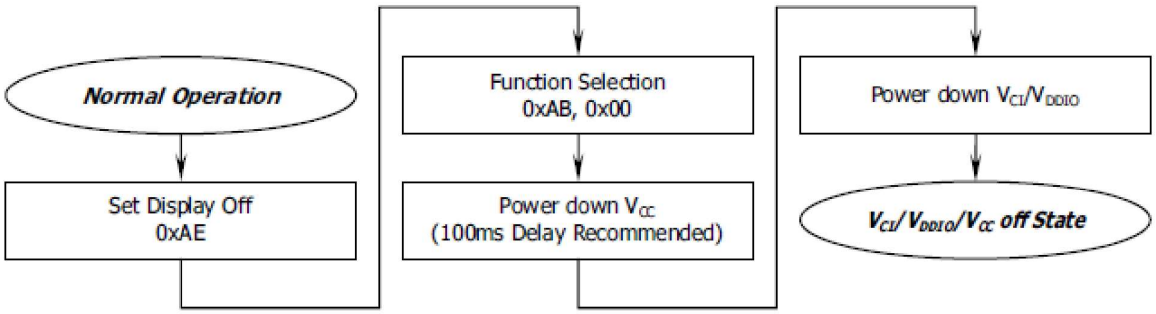
4.5.1 VCC Supplied Externally

<Power up Sequence>

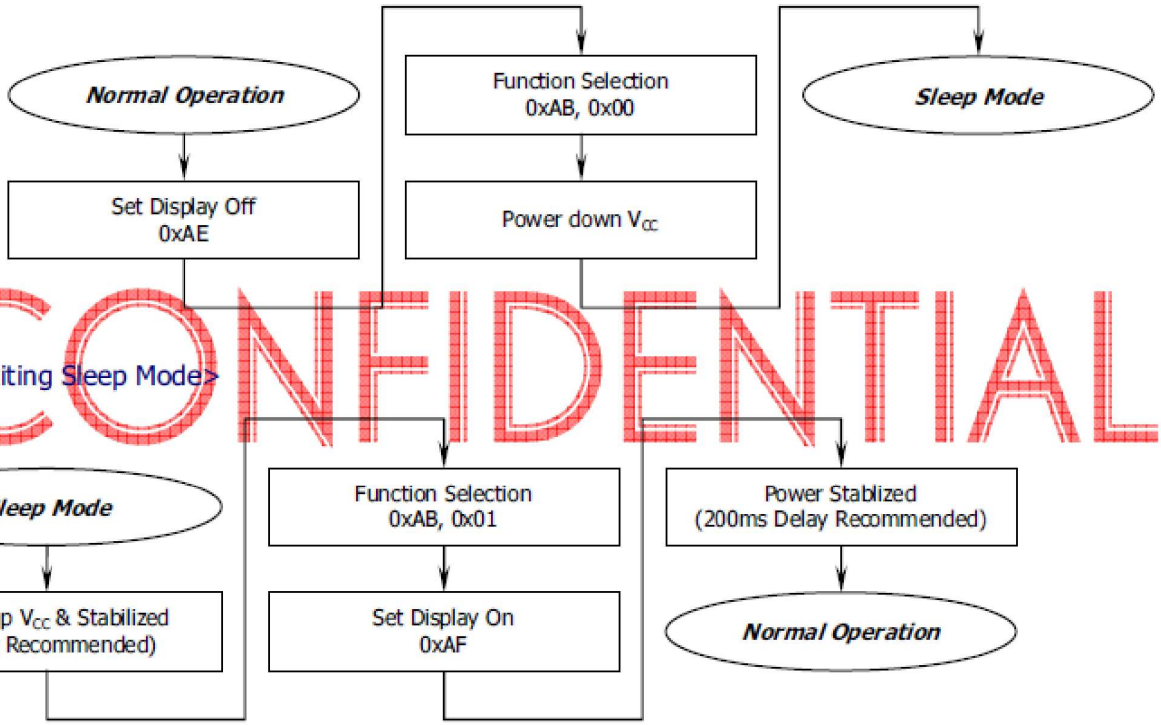


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	--
Operating temperature	T_{OP}	-20	+70	℃	--
Storage temperature	T_{ST}	-30	+80	℃	--

Notes

1. If used beyond the absolute maximum ratings, FT6436U may be permanently damaged. It is strongly recommended that the device

be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics,it may affect the reliability of the device.

2. Make sure VDDA (high) ≥VSSA (low).

3. Make sure VDD3(high) ≥VSS(low).

8.1.2 DC Electrical Characteristics

Table 3-2 DC Characteristics (VDDA=2.8~3.6V, Ta=-40~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 x IOVCC	V	

I/O leakage current	ILI	Vin=0~VDDA	-1	-	1	μA	
Current consumption (Normal operation mode)	Iopr	VDDA =VDD3= 2.8V Ta=25℃ MCLK=18MHz	-	4.32*1	-	mA	
Current consumption (Monitor mode)	Imon	VDDA =VDD3= 2.8V Ta=25℃ MCLK=18MHz	-	220*2	-	uA	
Current consumption (Sleep mode)	Islp	VDDA =VDD3= 2.8V Ta=25℃	-	55	-	uA	
Step-up output voltage	VDD5	VDDA = VDD3=2.8V	-	5	-	V	
Power Supply voltage	VDDA VDD3		2.8	-	3.6	V	

*1: Report Rate: 75Hz @ 4"TP

*2: Report Rate: 25Hz @ 4"TP

8.1.3 AC Characteristics

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V; Ta=25℃	34.64	36	36.36	MHz	

Table 3-4 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V; Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V; Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25℃	-	5	-	V	

8.2 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on.

INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

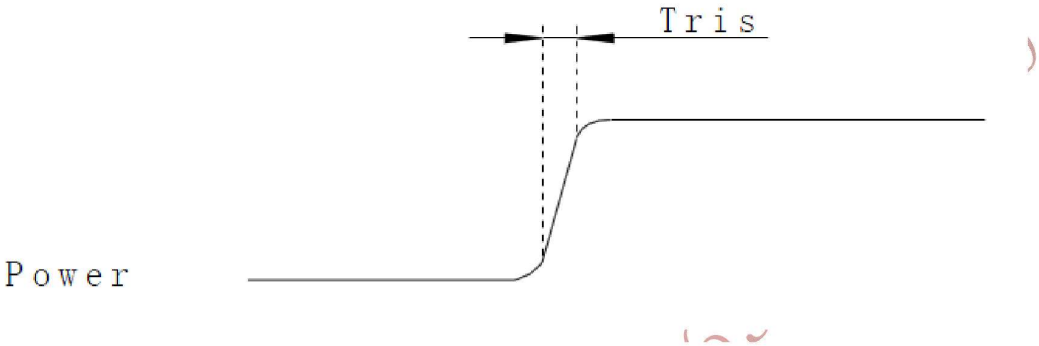


Figure 3-7 Power on time

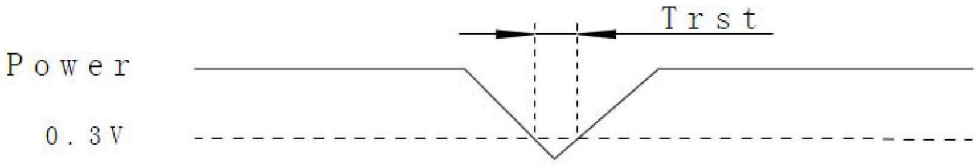


Figure 3-8 Power Cycle requirement

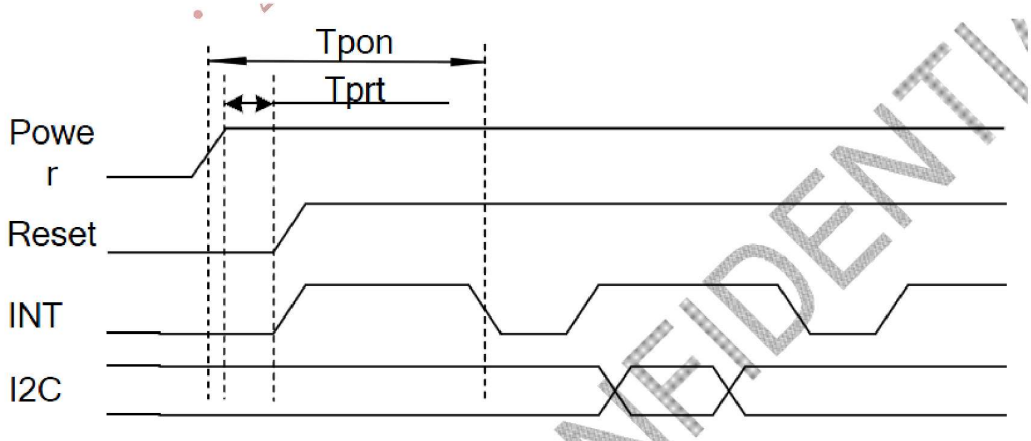


Figure 3-9 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

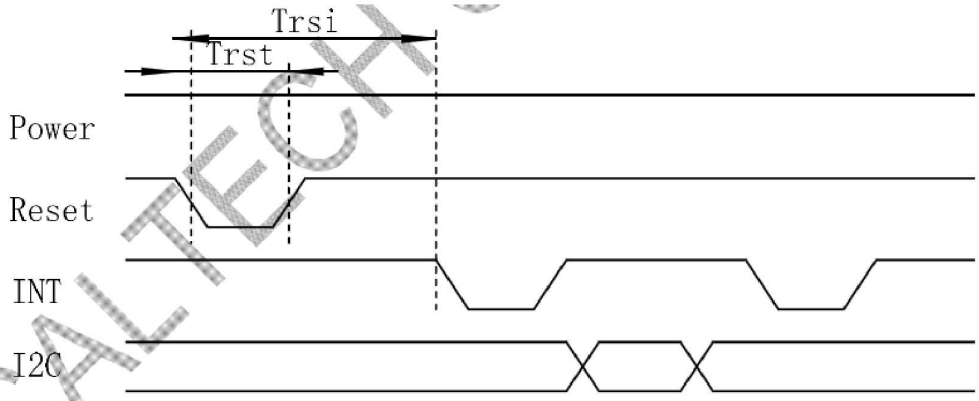


Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

8.3 Serial Interface

FT6436U supports the I2C interfaces, which can be used by a host processor or other devices

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

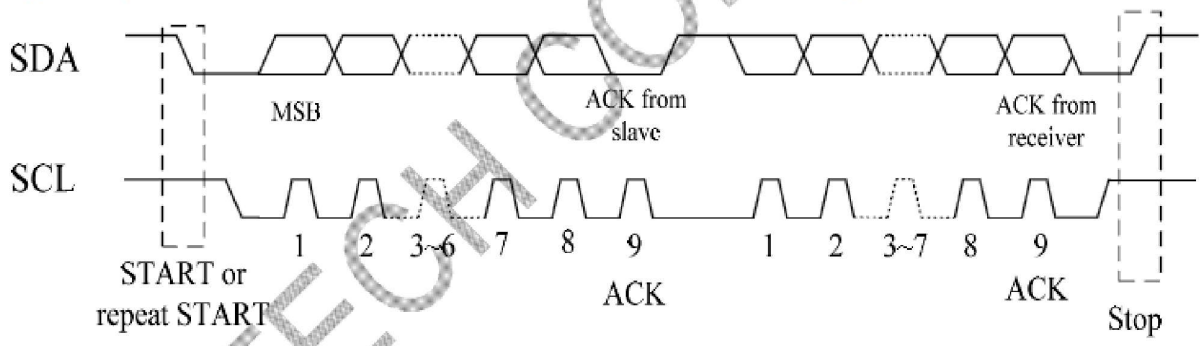


Figure 2-4 I2C Serial Data Transfer Format

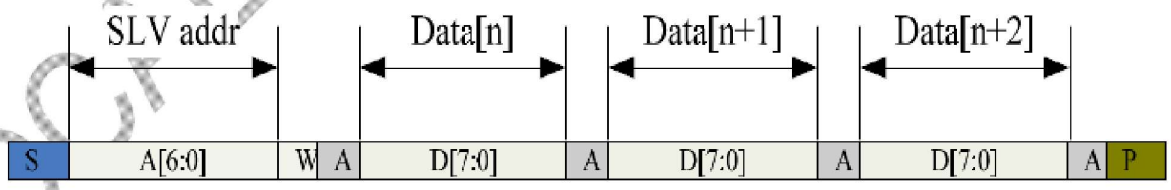


Figure 2-5 I2C master write, slave read

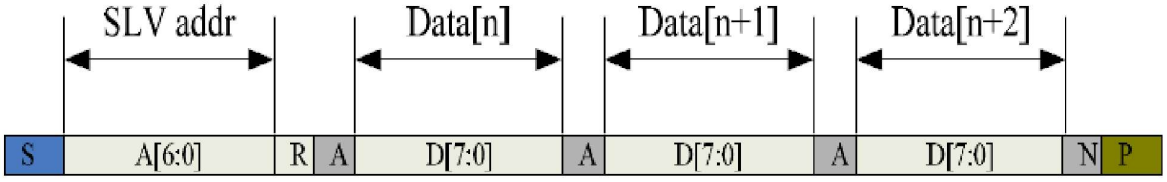


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

9. Appearance Inspection

9.1 Appearance Condition

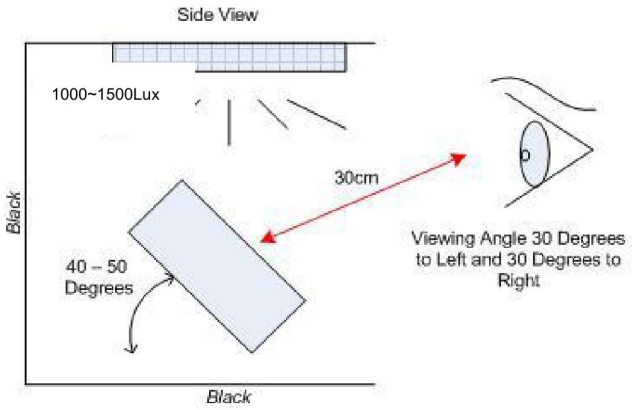
9.1.1 Environment: 22 ± 3ºC, Inspection distance：30 ± 5cm.

9.1.2 Rotation angle : ±45º

9.1.3 Lighting illumination：1000~1200Lux

9.1.4 Background：Black

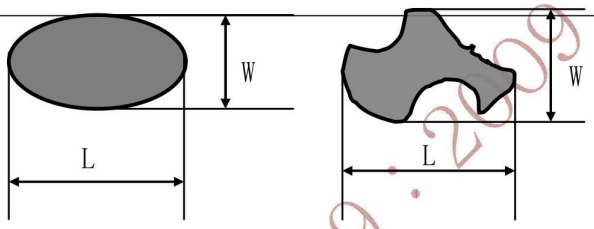
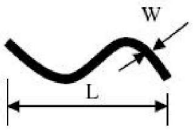
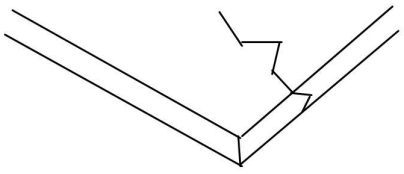
9.1.5 Inspection time：30s each piece



Remark:

Inspection criterions are valid for the complete Module (TP + OLED) including reverse Printing and Logo printing

9.2 Appearance Criterion

No.	Item	Criteria for defects (Unit: mm)
1	**Dot Defects (Particle/Dirt/ Dent/Bubble)**	1、D≤0.2 mm; Ignore 2、0.2 mm＜D≤0.5 mm,N≤5, Distance ≥70mm D≥5mm is not allowed. D=(W + L)/2 
2	**Line type Defects (Scratch/Dirt/Particle)**	1、W≤0.063mm , Ignore 2、0.063mm＜W≤0.1mm,L≤8mm(length in total),N≤4; Distance ≥70mm Other is not allowed. 
3	**Edge Chipping**	Allow: Edge Chips/chamfered Edges: Corner: D≤ 0.3mm Polished edges: D≤ 0.25mm, Ignore; 0.25mm<D≤0.4 mm,N≤5 per edge allowed Heat marks on polished edged: Width max. 0.15mm, length max.4.0mm. Max.2 per 500mm,min. distance>40mm
4	**Glass Crack**	Crack is potential to enlarge, any type is not allowed. 
5	No visible color change when compared with the approved sample	

Remark	For No.1.2 and 2.2 8 defects in total are allowed A concentration of defects is not allowed, definition in accordance with DIN ISO 10110-7

10. Reliability Test Result

10.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	−30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

12. Packing

----TBD----------